NASA SP-6509

TECHNIQUES OF FINAL PRESEAL VISUAL INSPECTION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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TECHNIQUES OF FINAL PRESEAL VISUAL INSPECTION

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GLOSSARY

Bimetallic	A metallurgical system consisting of two different metals.
Boat	The holder which is used to support semiconductor wafers during high temperature operations.
Chip	A piece of silicon wafer in which a transistor, or a whole integrated circuit, is contained.
Contact window	Opening which has been etched in the silicon oxide layer so as to allow ohmic contact to the underlying silicon.
Dangling bond	An unshared covalent bond which exists along the edge of a crystal structure.
Dice	(v) To break a silicon wafer into individual pieces. (n) Pieces of silicon wafer (plural of die—see die).
Die	Singular of dice, individual piece of silicon wafer in which a transistor, or a whole integrated circuit, is contained (see chip).
Epitaxial growth (epitaxy)	Process by which single-crystal material is grown *on top of* another single crystal.
Eutectic temperature	The lowest temperature at which a two-element metal system can melt.
Evaporation (vapor deposition)	Method of depositing one material on top of another. Atoms of the first material are boiled off of a heated filament and deposited on the second material. The process is carried out in a vacuum.
Interference colors	Color which appears in thin film as a result of destructive interference of the light waves as they are transmitted through the film and reflected back from the substrate.
Laminar flow hood	Hood in which exhausted air is uniform in its flow pattern, and which is relatively free of back-streaming contamination.

Photosensitivity	Property of a material whereby its chemical make-up is altered by exposure to light.
Scribing	Process in which a sharp diamond stylus is moved along a single-crystal silicon wafer, creating stresses in the crystal lattice.
Scrubbing	Process used during soldering in which one of the parts is rapidly moved across the other. The rubbing motion breaks up oxide formations.
Wafer	A slice of semiconductor material.

TECHNIQUES OF FINAL PRESEAL VISUAL INSPECTION

BACKGROUND

Space missions have always required reliable electronic parts. However, with the advent of longer missions, these requirements have become even more stringent and, often, more costly. Unfortunately, the quality and reliability has not always kept pace with the environmental requirements; and, as a result, most users of high reliability parts specify elaborate screening procedures. These additional process steps have increased the cost to three or four times that of off-the-shelf parts. The screening procedures are quite effective in removing many parts with certain built-in manufacturing defects, whether due to deficiencies in workmanship or design. However, a significant number of such parts escape these screens.

Failure analyses conducted at Goddard Space Flight Center (GSFC) have shown that a large percentage of those microcircuit failures caused by manufacturing defects are attributable to poor workmanship. The remainder are due to problems inherent in the manufacturing technology. Large percentages of poor workmanship problems have been noted by others as well (references 1 through 4). It appears that more control of manufacturing processes, more effective screening procedures, and constant monitoring of incoming products by users are needed.

Workmanship problems should be detected during the final preseal visual inspection; that is, during the last step in fabrication before sealing the device within the can. Here, each circuit (100 percent) is examined at magnifications ranging from 40X to 400X. From experience, it is obvious that not all of the devices with poor workmanship are removed and some devices find their way into high reliability procurements. There are several reasons for inefficient removal of questionable units:

(a) Despite the screening standards (for example, MIL-STD-883), there is not complete agreement between vendor and user on what constitutes a visual reject.

(b) The inspector at the final preseal visual station examines large numbers of devices and may become careless.

(c) The inspector is not always aware of the seriousness of evident imperfections, and/or does not ask for clarification if uncertain.

As a result, users of extremely high reliability material often perform their own final pre-seal visual inspection in addition to, or instead of, the normal vendor inspection. This necessitates that procuring agencies have personnel experienced and trained in the complexities of semiconductor fabrication and inspection. Unfortunately, there are insufficient qualified personnel. To alleviate this problem at GSFC, a course has been prepared to train a specialized cadre of personnel to perform visual examinations with a high degree of competence and to instruct project support personnel in the art of visual inspection. This text has been prepared as a training aid for the course.

INTRODUCTION

The normal process of microcircuit fabrication will be explained in this text. Each process step is described both as to its purpose and as to problems that may be introduced into the finished product.

The microcircuit manufacturing operation is divided into prepackaging and packaging operations (see figure 1). For monolithic integrated circuits, prepackaging concerns all those processes necessary to prepare the semiconductor material and create discrete microcircuits in the material. These microcircuits are then divided, mounted, and connected to the external leads of the package, and hermetically sealed during the packaging operation. For hybrid microcircuits, the discussion concerns those areas of fabrication which are unique to hybrid circuits (for example, thick and thin film resistor fabrication and capacitor fabrication).

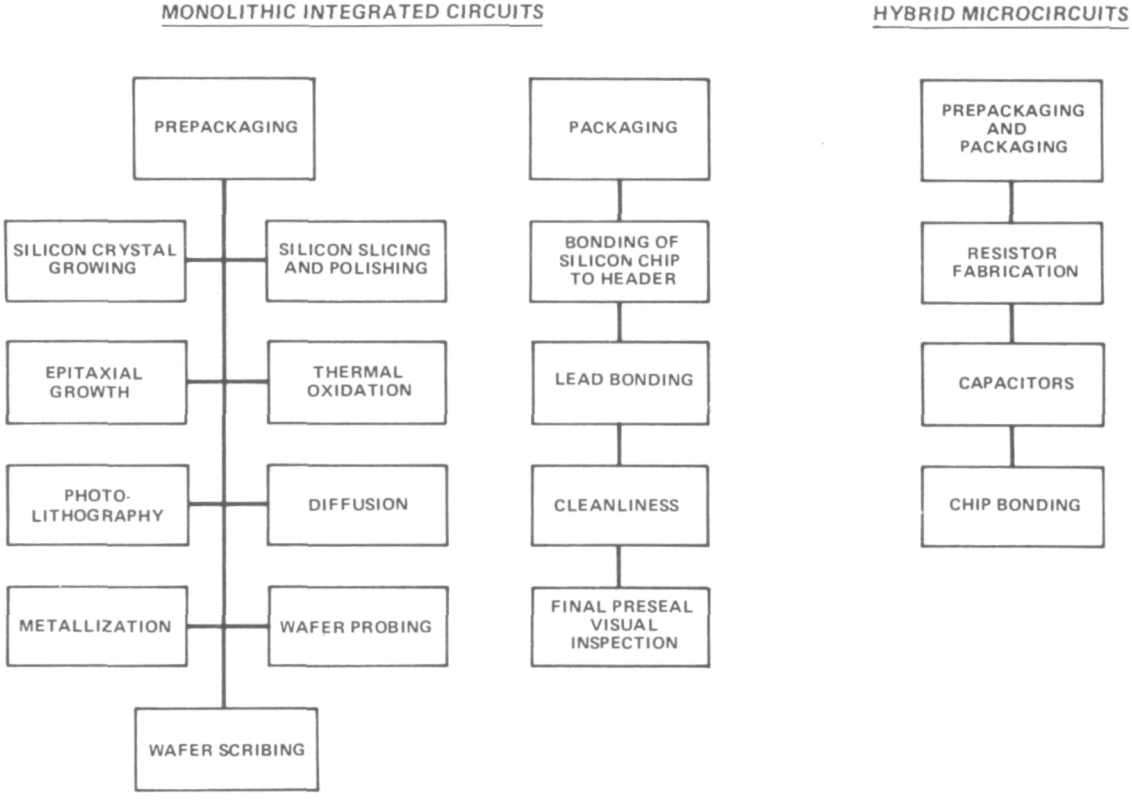


Figure 1. Microcircuit manufacturing operations.

The manufacturing operation is far more complex than this description; more than 100 process steps are required to fabricate a typical microcircuit. If each stage is examined, however, it is seen that, particularly in the prepackaging phase, a number of the processes are repeated as many as four times during the operation. We need only relate to the basic process to demonstrate the correlation of process to failure mechanism.

The ensuing discussion describes the basic processes and illustrates typical failures resulting from fabricating problems. Where possible, photographs of actual anomalies are given as well as applicable accept/reject criteria for these anomalies excerpted from screening standards:

MIL-STD-883, Method 2010.1 (Final Preseal Visual Inspection)

Marshall Space Flight Center 85M03924 (Internal Visual Inspection of Transistors, Standard For)

PREPACKAGING TECHNIQUES

Silicon Crystal Growing

Technology

Integrated circuits and hybrid microcircuits are based on grown single crystals, usually of silicon. Cylindrical silicon rods, 2.5 to 5 cm (1 to 2 in.) in diameter, are grown to lengths of 15 to 30 cm (6 to 12 in.) in high temperature, vertical furnaces as seen in figure 2.

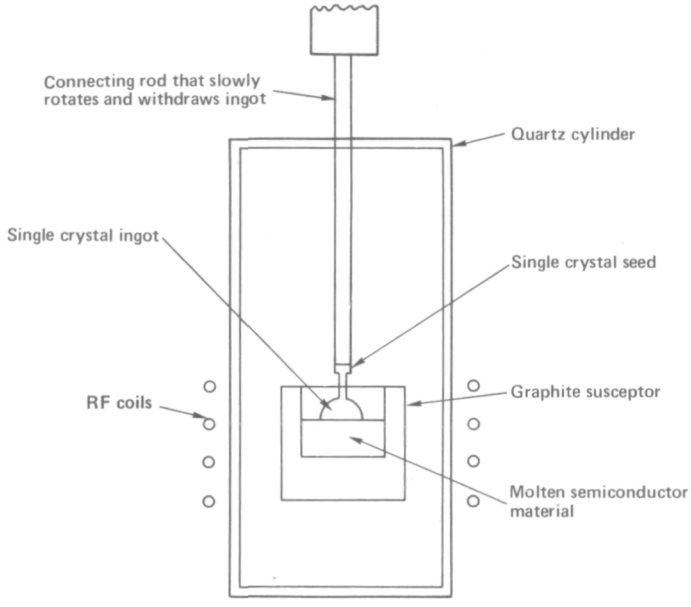


Figure 2. Vertical furnace used for growing semiconductor single crystals.

During crystal growth a controlled amount of a chemical element (usually phosphorus or boron) is introduced into the silicon to produce its electrical conductivity characteristics. Care must be exercised to control the purity of all materials in the furnace (reference 5), the uniformity of the silicon's electrical resistivity, and the degree of crystalline imperfection in the silicon rod.

Failure Mechanisms

Variations in uniform resistivity primarily affect the manufacturer's yields by causing changes in the device parameters. Crystalline imperfections, because of their effect on

subsequent high temperature diffusion processes, where they directly influence diffusion parameters, also affect yield (reference 6). Noncatastrophic failures due to this type of defect are difficult to screen, since they are by nature time dependent. Etch pits are sometimes visible (figure 3a); however, unless these etch pits cross a junction, as shown in figure 3b, they should not be considered cause for rejection.

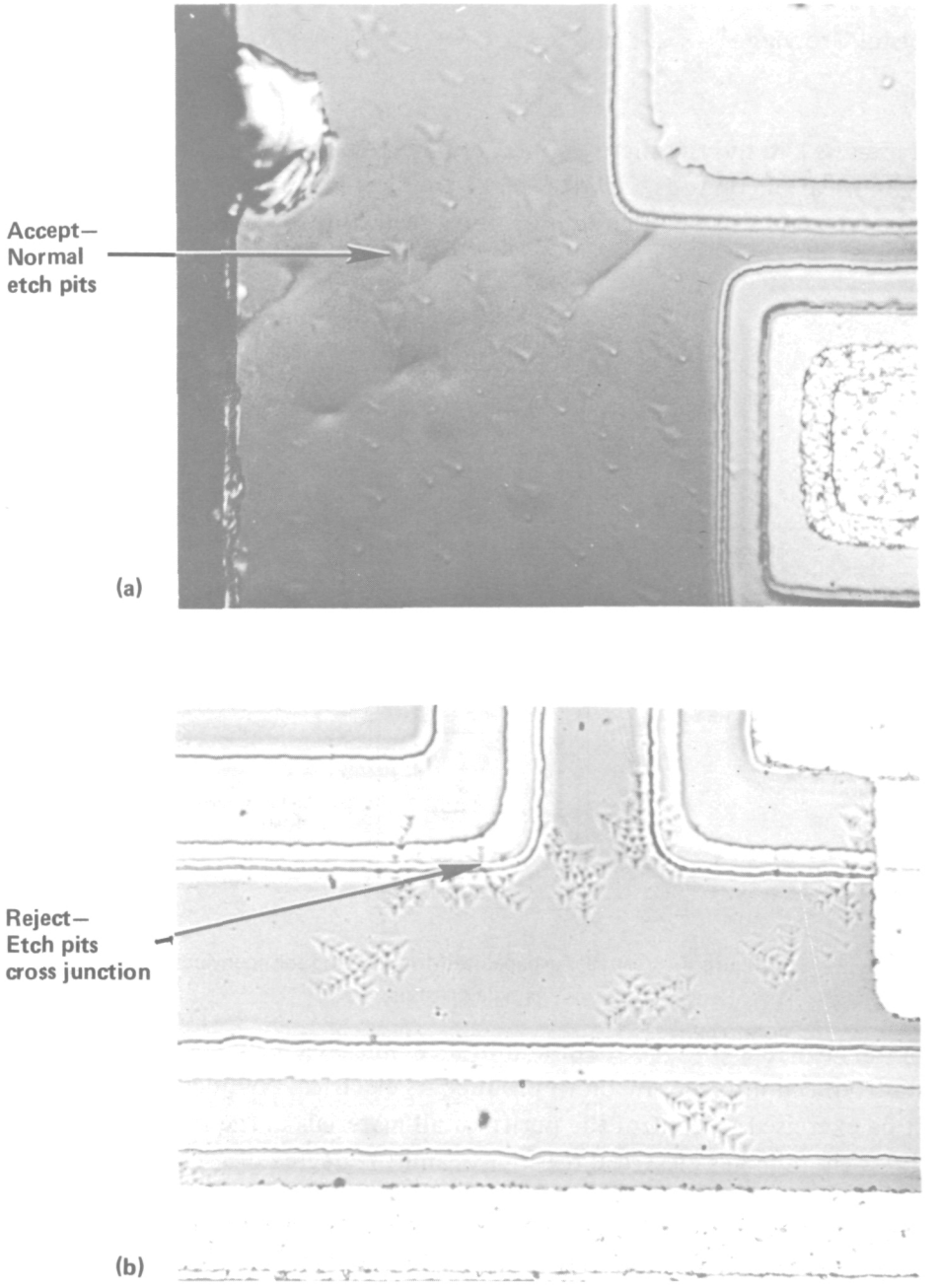


Figure 3. Imperfections in crystal structure, 400X magnification.

Silicon Slicing And Polishing

Technology

Wafers are sliced from the silicon rod with diamond-edged wheels or wires. After cutting, the wafers are approximately 2.5×10^{-2} cm (10 mils) thick and are mechanically lapped and polished to a final thickness of approximately 1.2 to 1.8×10^{-2} cm (5 to 7 mils) (figure 4).

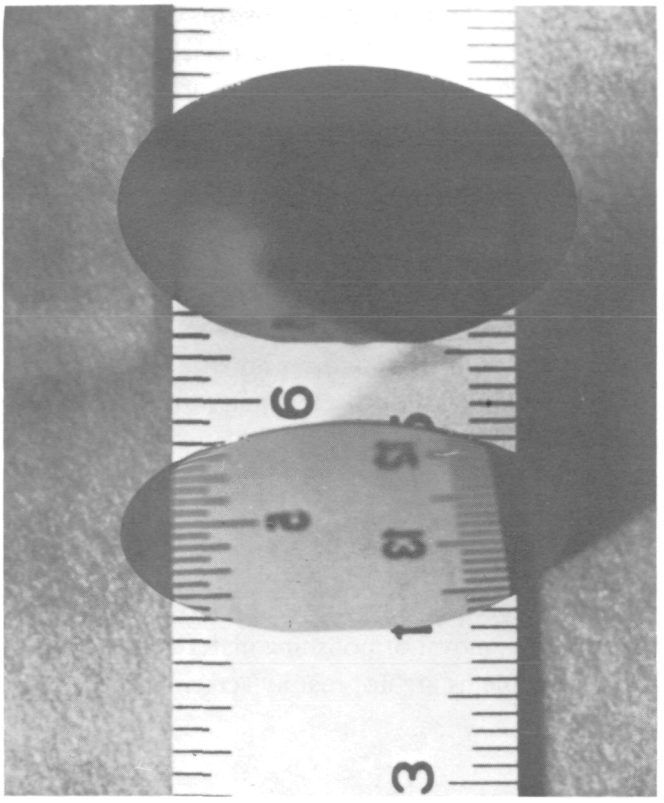


Figure 4. Lapped wafer (top); lapped and polished wafer (bottom).

During these finishing operations, successively smaller abrasive size particles (ranging from 5 to 0.05 μm) are used until a mirror finish is obtained. The abrasive is usually aluminum oxide or zirconium oxide mixed with deionized water. As in any polishing operation, care must be exercised to prevent unwanted scratches. Certain types of surface scratches may be prevented by maintaining separate rooms, areas, or laminar flow hoods for each abrasive particle size used. This reduces the possibility of a large particle contaminating a wafer surface during subsequent polishing with a smaller sized particle.

Mechanical polishing introduces strains and mechanical damage in the polished surfaces (reference 7), which affect the following epitaxial growth and diffusion processes in a manner similar to crystalline imperfections in "Silicon Crystal Growing" above. Mechanical damage must, therefore, be removed by etching. Acids such as hydrofluoric (HF), nitric (HNO_3), and glacial acetic (CH_3COOH) are used in various combinations.

Finally, after the slices are etched, they must be thoroughly rinsed. For rinsing, solvents such as acetone, ethyl alcohol, and trichloroethylene are used. Occasionally a followup rinse of HF and then a deionized water rinse is made. Stains, films, organic matter, and metal ions cannot be tolerated on the wet surfaces, as this contamination will also affect subsequent operations. Ideally, the solvents, acids, other chemicals, and water used during this processing stage and all other stages of the manufacturing operation should be 100 percent pure. Purity control of chemicals and water to the degree demanded in microcircuit technology is difficult to maintain. Slight variations (for example, the introduction of a few parts per million of unwanted impurities) sometimes produce low manufacturing yields and latent device failures.

Failure Mechanisms

Areas on the silicon wafer with mechanical damage are attacked faster by the etches than are undamaged areas. This etching permits discrepancies to be readily screened during visual inspection and are identical to the etch pits of figure 3. Problems related to the etching are usually manifested as an orange peel ripple surface (figure 5). Surface ripple is not considered cause for rejection.

Contamination will ultimately cause lower yields during manufacturing and produce reliability problems similar to those produced by crystal imperfections. The foreign matter may originate from incomplete removal of polishing material or be introduced during polishing or etching. These problems are not readily screened.

Epitaxial Growth

Technology

Epitaxial growth, or epitaxy, involves the growth of a new layer of silicon upon the parent silicon wafer, such that the new layer becomes an extension of the atomic crystal lattice structure in the wafer. The new layer differs from the original wafer, however, in either its resistivity value and/or conductivity type.

Epitaxial growth is accomplished in a horizontal furnace (figure 6). The silicon wafer is heated on a silicon monoxide-coated graphite block ("boat" in semiconductor vernacular) inside a high-purity quartz tube. A radio frequency (RF) coil is positioned outside the tube and around the site at which the boat is located. The slice is initially heated and then etched by allowing a mixture of hydrogen chloride (HCl) vapor and hydrogen (H_2) to flow over it. The etching is stopped and the epitaxial process then begins with the introduction

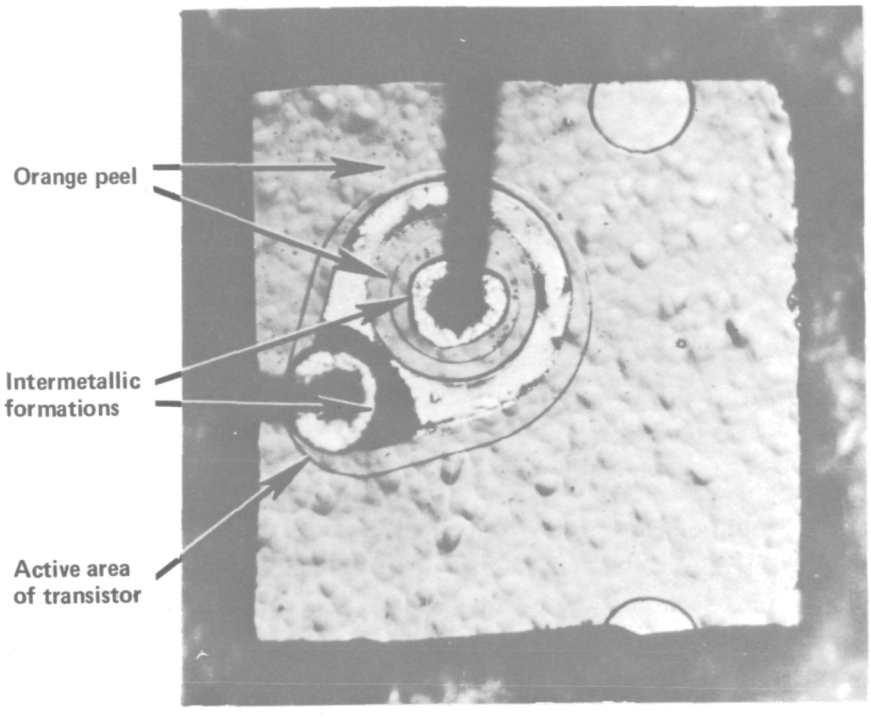


Figure 5. Orange peel surface.

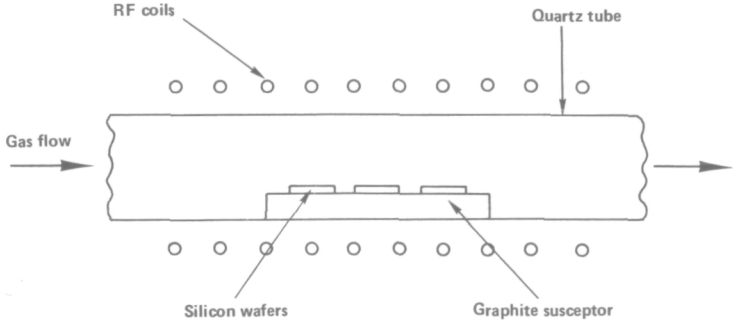


Figure 6. Horizontal furnace used for growing epitaxial layer.

of silicon tetrachloride ($SiCl_4$) vapor and H_2. The $SiCl_4$ decomposes while flowing over the hot silicon wafer and deposits silicon (Si) on the wafer. (An additional element, in gaseous form, is usually added to the H_2 and $SiCl_4$ in order to control the resistivity and conductivity of the epitaxial layer). In most cases, boron (B) or arsenic (As) is added by introducing either diborane (B_2H_6) or arsine (AsH_3). These decompose in a manner similar to $SiCl_4$, yielding free boron or arsenic.

There are many controls important to the success of this process:

1. The perfection of the parent silicon wafer's crystalline structure and the cleanliness of the wafer surface
2. The absence of dust or other contamination on the surface of the silicon wafer
3. The purity of all materials in the furnace tube
4. The flow rate and composition of the gas mixtures
5. The temperature uniformity

Failure Mechanisms

Controls 1 and 2 would be those most concerned with reliability, as the other factors would more adversely affect the manufacturer's output. Imperfections in the parent crystal, scratches on the wafer surface, and surface contamination such as dust produce defects in the epitaxial layer (reference 8). These small defects, termed stacking faults, are usually manifested as triangular etch pits (again similar to the crystalline faults in "Silicon Crystal Growing"). Defects of this nature often cause latent failures in microcircuits. Unless serious degradation has taken place at an epitaxial defect site, the defect will escape detection during tests imposing normal electrical voltages. In a finished device, these defects are extremely difficult to detect.

Thermal Oxidation

Technology

Silicon dioxide (SiO_2) is grown on the silicon wafer to act as a mask to diffusing elements later introduced and as a final protective layer over components of the circuit produced in the silicon chip. The wafer is heated to a very high temperature, 1175 to 1475 K (900 to 1200° C), inside a high-purity quartz tube mounted in a horizontal furnace (figure 7). The wafer(s) rests on a quartz boat, and either oxygen (O_2) gas, or a combination of oxygen and nitrogen which has been passed through steam, is allowed to flow over the wafer. The thickness of the resultant SiO_2 on the wafer is controlled by the time and temperature of the process. This oxide growth has a parabolic time dependence and can be controlled with extreme accuracy. Since the oxide films used on semiconductors are very thin, on the order of 0.1 to 1.0 μm (1000 to 10,000 Å), and since the original polished surface of the underlying silicon interface is mirror-like, the oxide films display interference colors. These colors are brilliant and can be used to judge the thickness of the oxide or variations in the thickness. Figure 8 is an optical photograph of a transistor and shows variations in contrast related to differing interference colors.

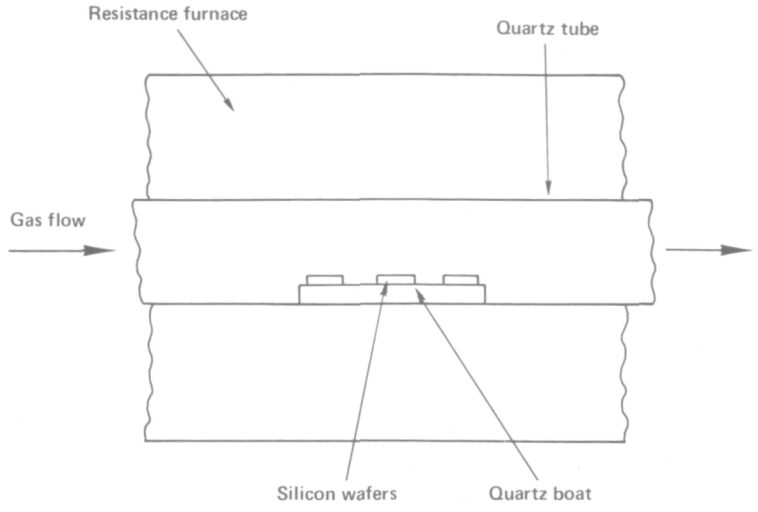


Figure 7. Horizontal furnace used for oxidation and diffusion.

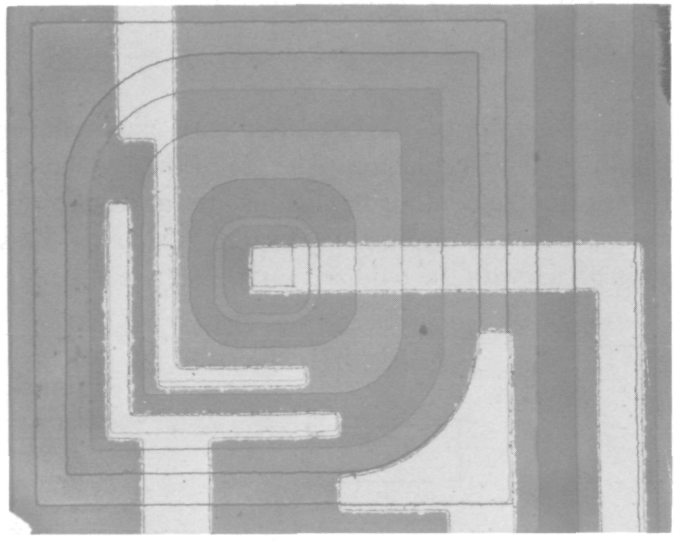


Figure 8. Various interference colors in silicon oxide layer.

Failure Mechanisms

There are many unanswered questions concerning the effects of impurities in the SiO_2 on the electrical characteristics of a device. Therefore, the purity of all materials used in the oxide processing step is of great importance. In addition, it has been postulated that defects exist in the oxide because of the nature of its atomic bonding with dangling silicon atoms at the surface of the silicon wafer. Surface treatment of the silicon wafer before oxide growth also affects the resultant oxide. In addition, the presence of mobile sodium (Na^+) and less mobile hydrogen (H^+) ions in the oxide has been detected, and these ions

redistribute themselves within the oxide under the influence of electrical fields or heat energy (references 9 and 10). When a layer of the ions (usually Na^+) accumulates on the surface of the oxide, an opposite charge layer is created in the silicon just below the silicon-silicon dioxide interface. The charge layer may produce a conductive channel which can cause unwanted current leakage across a diffused, electrical junction.

During the fabrication of the desired circuit within the silicon, a number of oxidation steps are performed. High reproducibility from one oxidation to the next is necessary in order to avoid oxide-etching anomalies during the photolithographic operation.

It is essential that the silicon surface be free of dust and other contamination before oxidizing, otherwise pits and holes in the oxide will result. Defects produced during this process can be readily diagnosed while the material is still in the virgin wafer state. These problems are often demonstrated by irregularities in the color of the oxide, pips or bumps in the surface, and so on. (Problems relating from charge buildup can only be detected by sophisticated techniques or by electrical measurements of the devices fabricated from the material.) However, after subsequent fabrication steps, changes in oxide coloration may be masked and the possibility of detecting flaws is minimized.

Photolithography

The fabrication of silicon planar devices has been, to a great extent, dependent upon the development of photolithographic techniques. The use of these techniques has enabled device designers and fabricators to continually diminish the areas of both the active parts and the metallization stripes interconnecting these parts. A step-by-step sequence is shown in figure 9. The process begins with the oxidized surface (figure 9(a)).

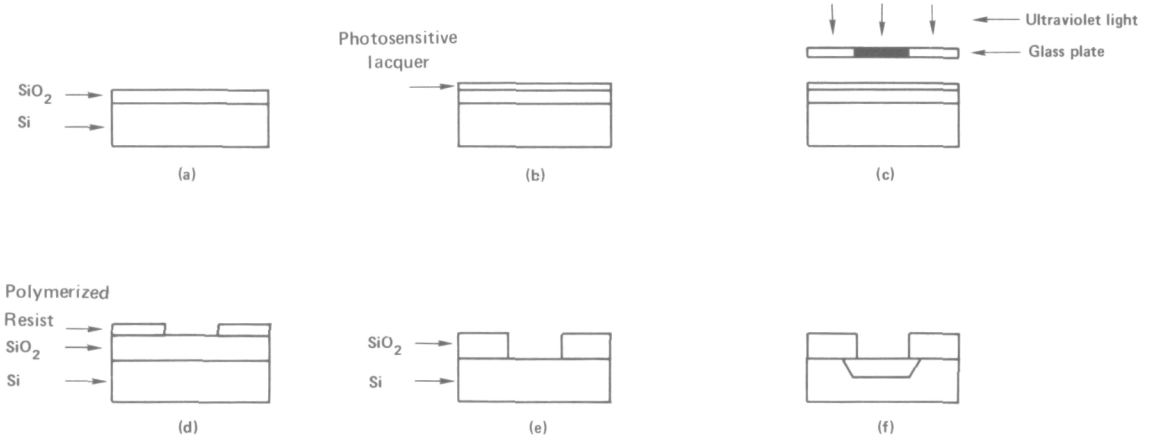


Figure 9. Photolithographic process steps.

A thin layer of photosensitive resist is applied over the oxidized silicon wafer (figure 9(b)) and exposed to ultraviolet light (UV) (figure 9(c)). The pattern of exposure is determined

by "windows" in an opaque pattern on a special glass plate which is placed in intimate contact with the dried resist. (The pattern might be a matrix of transistor collector, base, or emitter diffusion windows, or perhaps of metal-contact evaporation windows.) Resist which is exposed to the ultraviolet light is polymerized and is not affected by chemical developing. Unexposed resist is soluble in the developer and is thus removed during developing. After the resist is exposed, developed (figure 9(d)), and cured in an oven at 373 to 443 K (100 to 170° C), the silicon dioxide is etched (figure 9 (e)). During chemical development, the unexposed resist (areas which correspond to and were under the opaque pattern) is removed, thereby exposing the material to be etched. Finally, the polymerized lacquer is stripped and the wafer is cleaned. The wafer is now ready for any subsequent process; for example, diffusion (figure 9(f)). This entire process may be repeated as many as four or five times for the various diffusions which take place, and again for creating the metallized contacts and interconnections. Each time another photolithographic step is performed the new pattern must be precisely aligned within each of the previous patterns over the entire matrix.

A short book could be written on the photolithographic process and the attendant problems. A considerable amount of information on the process and its control has been published in the past several years, and references 11, 12, and 13 are suggested for those seeking more detail. It should then suffice to briefly summarize the materials used and the controls necessary.

Process Steps and Materials

Application of lacquer – Most commonly employed are the photo resists made by Eastman Kodak. The resists are polyvinyl alcohols which are polymerized upon exposure to UV light or heat.

Development of lacquer – Kodak Photo Resist Developer, trichloroethylene, or xylene.

Etching of silicon dioxide – Hydrofluoric acid, water, and ammonium fluoride.

Stripping of lacquer – Eastman has listed as many as 58 different chemicals for this task. Bell Telephone Laboratories has used triethylenetetramine (Trien) successfully. More often, hot sulfuric acid, hot nitric acid, a mixture of both, or a commercial stripper is employed.

Cleaning of silicon wafer (except for a metallized wafer) – The wafer is etched in a weak hydrofluoric acid immediately following a diffusion, rinsed in deionized water, and then rinsed in ethyl alcohol, before applying the new resist layer. This procedure is usually followed for the very first application of photo resist, also.

Process Controls

1. Polymerized particles in the photo resist must be carefully filtered out before application of the resist to the silicon wafer.

2. The surface of the silicon wafer to which the resist is applied must be thoroughly clean, dry, and dust-free.

3. All solutions used to rinse or clean the silicon wafer must be thoroughly filtered to remove particulate matter.

4. Tight control over the viscosity of the photo resist must be maintained, and uniformity and control of the thickness of the applied layer of resist on the silicon wafer is necessary.

5. The photolithographic mask pattern must be perfect and the glass plate upon which it has been created should be free of dust and scratches.

6. Application of the photo resist, mask alignment, and exposure should be done in a controlled environment that is both dust-free and dry and has little variation in room temperature.

7. Registration of a mask pattern inside of a previous pattern must be precise and accurate.

8. All photo resist must be completely removed after each photolithographic operation.

9. Handling of the silicon wafer must be such that no contact is made with the area of the photo resist to be exposed or developed.

10. Care must be exercised to regulate the UV light exposure time during pattern exposure and the etch time when etching an oxide diffusion window.

Failure Mechanisms

Photolithography is one of the most demanding and difficult processes in the production of microcircuits. It is not uncommon to see poor production yield at this point of the operation or many subsequent failures produced by defects introduced during the photolighographic process. Very careful visual inspection can reduce a number of the faults which could work their way down the production line and eventually out the shipping door. From a practical or economical standpoint, however, it is an almost impossible task to perform effective, 100 percent visual screening after each photolithographic step with the inspection instrumentation presently utilized. Therefore, only sampling inspection is performed. Rejection criteria are usually based on a set of typical defects resulting from weaknesses in the controls previously described. Many escape detection, and a subsequent visual examination (for example, final preseal visual inspection) hopefully weeds those out. Photolithographic defects, which finally get through all manufacturing tests and inspections, commonly cause latent failures in microcircuits and can sometimes be recognized only after arduous screening. The most prominent causes of latent failures have been current leakage or electrical shorts through pinholes in the oxide, current leakage across photo resist bridges between metallic contacts or interconnections, current leakage along a fault in the silicon dioxide boundary, and diffusion pipes (reference 14) producing low voltage breakdown or collector-to-emitter shorts. Pinholes are mainly traceable to failure of process controls 2, 3, 4, 5, and 6. Atoms of metal from a metal interconnection over an oxide

pinhole may, after a period of time, migrate through the pinhole to the silicon underneath. The migration takes place under the influence of an electric field between the silicon and the interconnection or by concentration diffusion. In either case, a short between the interconnection and the silicon occurs.

Photo resist bridging is caused by improper regulation of controls 1, 4, 5, and 8. Improved versions of photo resist (Kodak KTFR) are not hydroscopic, but evidently residual deposits of the resist act as nuclei for condensation of residual moisture inside a sealed package, and conductive paths result. It is also possible that such residual photo resist deposits could become conductive by the diffusion of elements introduced during the diffusion process into the deposits. The former effect has been the predominant type of failure mechanism observed, since more failures of this type have been found from condensation during low temperature tests.

Problems with controls 2, 4, 6, 9, and 10 primarily cause lifting or peeling of the resist from the silicon dioxide and also cause exposure irregularities; for example, the projection of a border of an oxide diffusion window for a transistor emitter across the base of the transistor into the collector. Obviously, a collector-to-emitter short would be manifested. Suppose, though, that the emitter border projected across the base and stopped within the base at a point extremely close to the collector border. The probability of this defect contributing to a latent type of collector-to-emitter failure is high, but in a sealed package the defect would elude detection by normal tests.

Diffusion pipes are related to controls 1, 2, 3, 5, 6, and 8. The pipes are created during diffusion either by the aggregation of atoms of the diffusant at nucleation sites formed from dust, photo resist, or other particulates, or by masking or subsequent diffusion by the particles. In the former case, the concentration of diffusant is highest at these sites, the concentration gradient is highest, and a deeper diffusion (in a highly localized region) occurs than elsewhere along the normal plan of diffusion. In the latter case, the result is a pipe of low concentration under the particle. The defect is one that is not always revealed by typical electrical testing and will degrade the characteristics of a component in the microcircuit after an unpredictable number of hours of operation.

MIL-STD-883 lists a number of rejection criteria. Principal among these are:

- Any pinhole that occurs on an actual junction area (figure 10).
- Any defect that reduces metallization to one-half of the designed metallization width, due either to photolithography or scratches in the metallization.
- Any defect that causes any diffusion area to be discontinuous (figure 11).
- Any defect that reduces spacing distance to less than one-quarter of the designed separation (figure 12).
- Any defect that connects two metallization stripes, due either to photolithography or scratches in the metallization (figure 13).

Some representative examples of the problems related to improper control of the photolithographic process are as follows:

Figure 10 shows a pinhole in the oxide which could cause current leakage problems. The pinhole is located directly over a junction.

Figure 11 shows a fault in the oxide profile which results from a flaw in the photolithography prior to an oxide-etch step. The result here would be either a direct short or a potential short between a diffused resistor and an isolation region.

Figure 12 shows an improper spacing in the metallization resulting from a flaw in the photolithography prior to metal etching. This narrow separation increases the possibility of electrical shorts due to small particles.

Figure 14 shows a large void in a metallization stripe. This void occurred as a result of some problem in the photolithography, such as dust or a scratch in the photo resist.

Figure 15 shows a device in which two exposure masks were misaligned. Unless severe, misalignment is extremely difficult to see. In this case, it caused catastrophic failure.

Figure 16 shows a device in which a contact window has incomplete metal coverage. (MIL-STD-883 requires 75 percent coverage of the window). This lack of coverage minimizes contact area and also increases the chance of lateral undercutting of the metal contact.

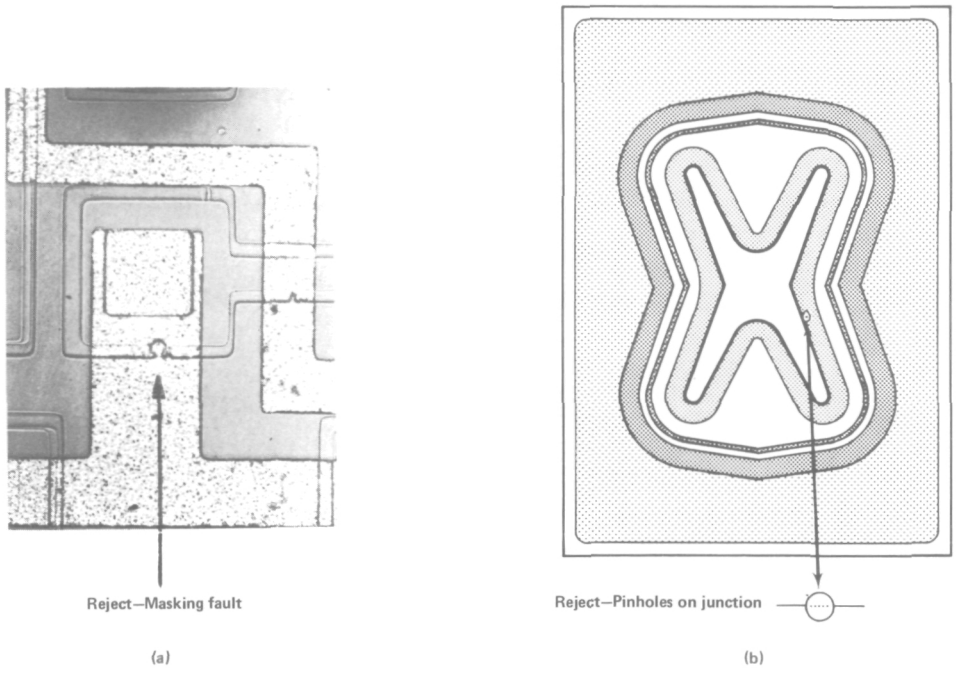
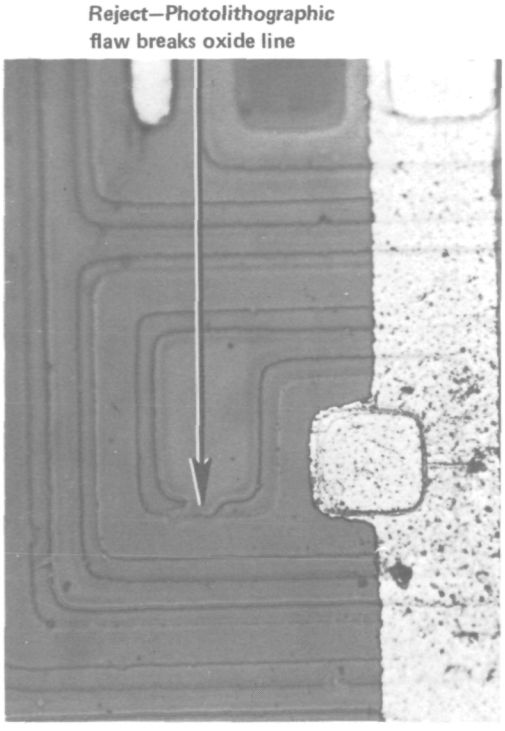
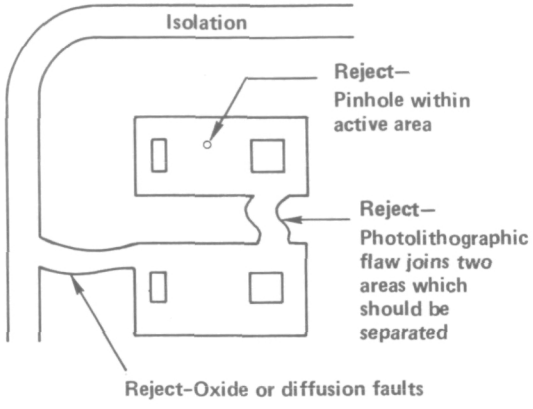


Figure 10. Photolithographic fault, pin-hole.
(a) Optical photograph; (b) Visual inspection criteria.

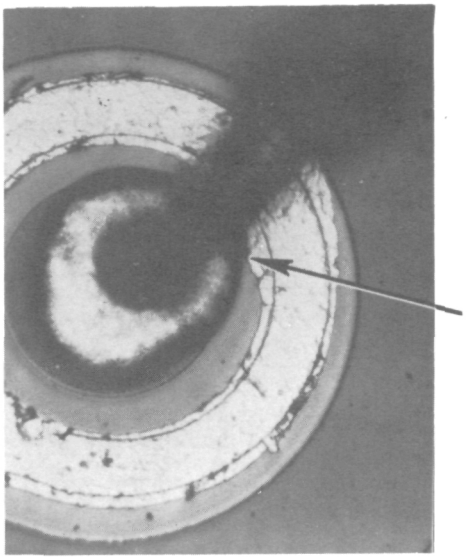


(a)



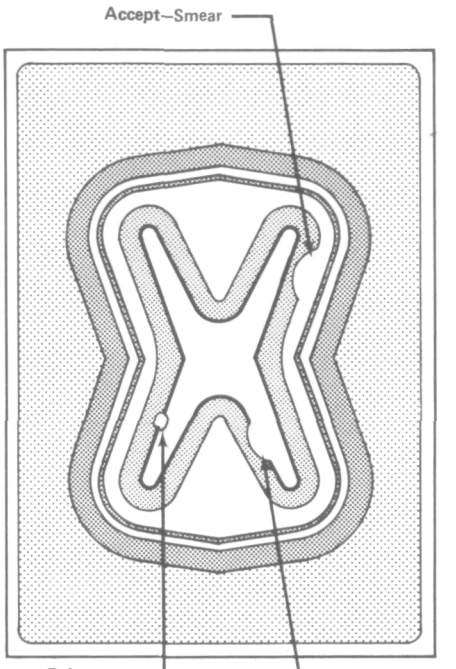
(b)

Figure 11. Photolithographic fault, discontinuous pattern in silicon dioxide.
(a) Optical photograph; (b) Visual inspection criteria.



Reject—
Spacing between
base-contact
metallization and
emitter ball bond
is in the order
of 2 μm
(0.00008 in.).

(a)



(b)

Figure 12. Photolithographic fault, improper spacing in metallization.
(a) Optical photograph; (b) Visual inspection criteria.

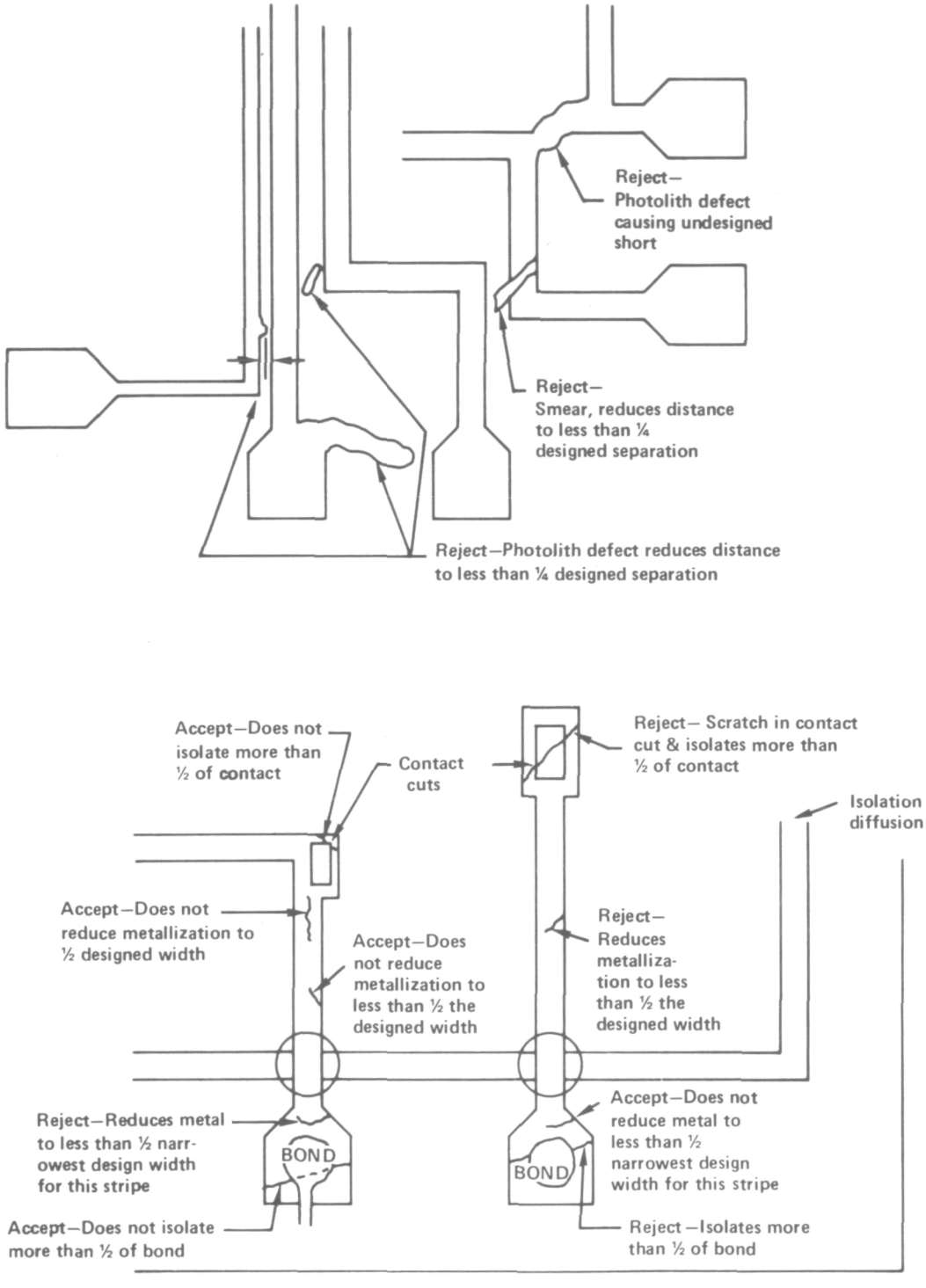


Figure 13. Scratches in metallization stripe, visual inspection criteria.

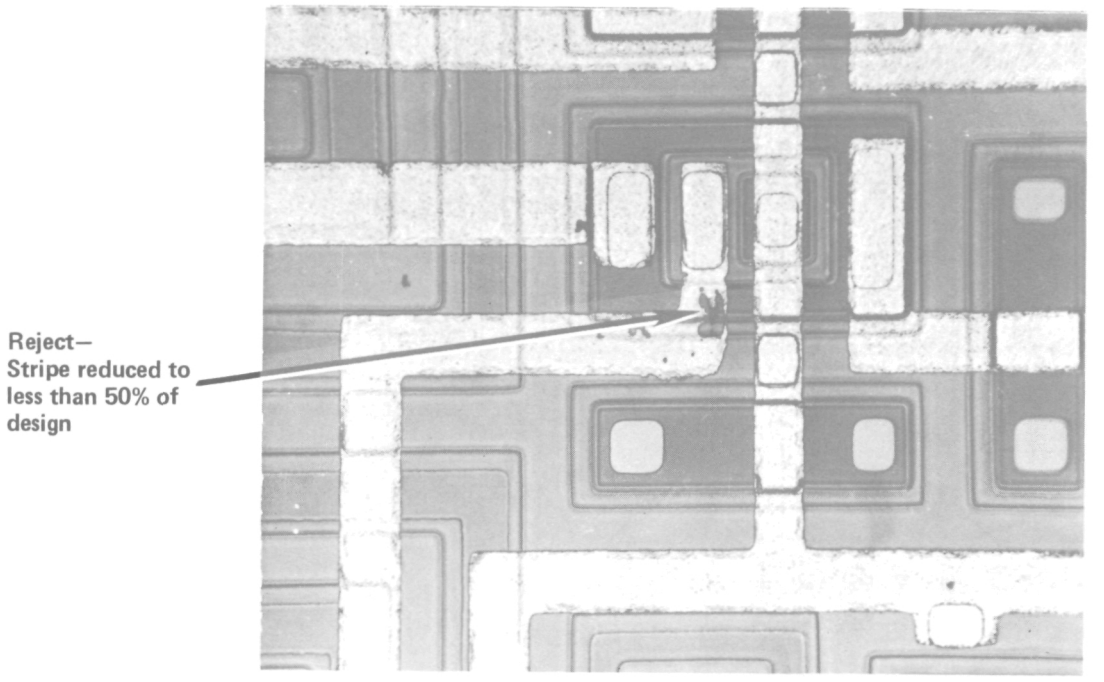


Figure 14. Photolithographic fault, reduced metallization stripe.

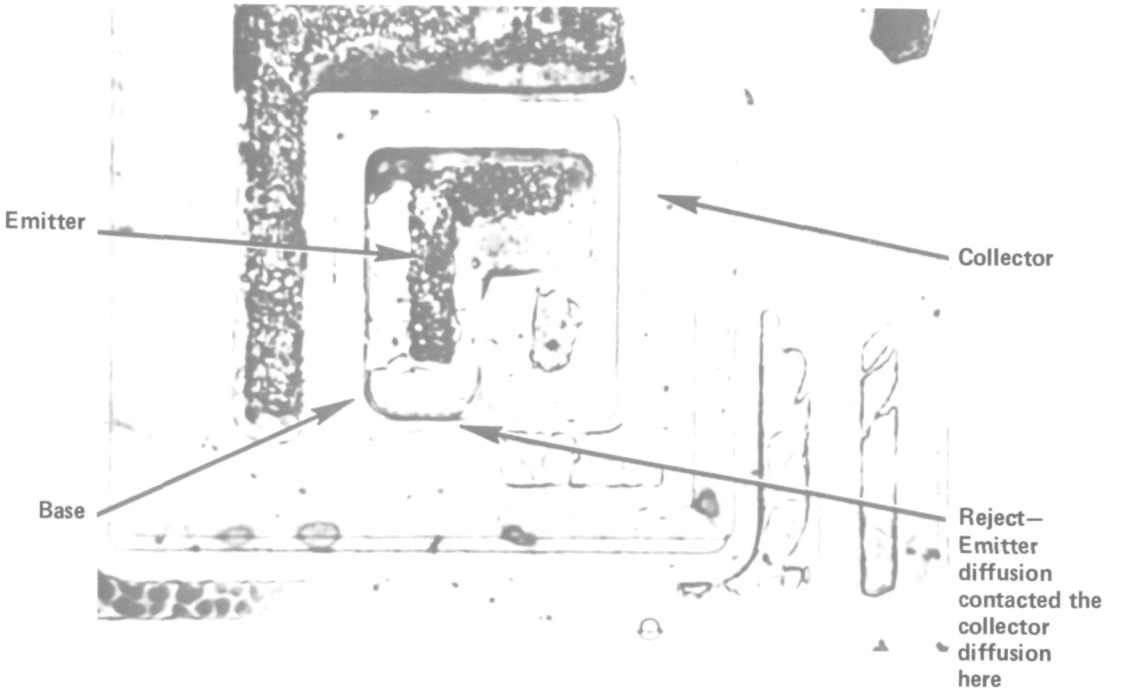


Figure 15. Misaligned transistor, emitter shorted to collector.

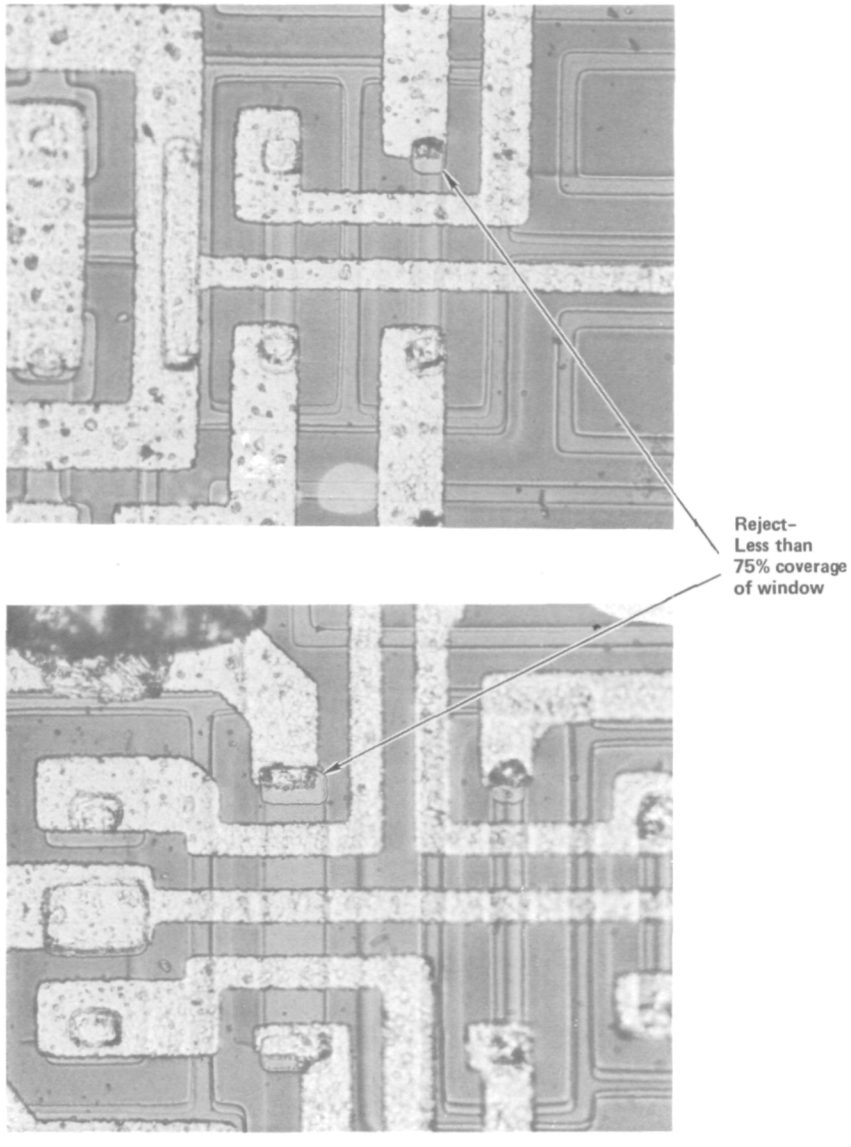


Figure 16. Incomplete coverage of contact windows.

Diffusion

Technology

The physical arrangement of equipment, material, and the process controls are basically the same as described in the section on oxidation. Oxidation is a one-step operation, whereas diffusion more often employs two steps (reference 14). The diffusing element is first deposited (predeposition) as a highly concentrated, extremely thin layer on the silicon wafer. The resulting layer is glassy and covers the exposed side of the silicon wafer. Slight diffusion of

the layer into the silicon also takes place where the silicon is exposed by the oxide diffusion windows. The remaining diffusant in the oxide windows is diffused deeper (drive-in) into the silicon at a higher temperature, 1375 K (1100° C), simultaneously producing a new oxide layer for the next diffusion. Typical elements diffused into the silicon are boron, phosphorous, antimony, and arsenic. The elements are derived from high temperature decomposition of vapors of boron oxide (B_2O_3), boron trichloride (BCl_3), boron tribromide (BBr_3), phosphorus oxychloride ($POCl_3$), stibine (antimony hydride - SbH_3), or arsine (arsenic hydride - AsH_3) as they are passed through the furnace tube over the silicon wafer.

Diffusant concentrations and diffusion depths are controlled by temperature and length of time of predeposition and/or drive-in; gas flow rate; and the diffusant source-gas plus carrier-gas (nitrogen, hydrogen, or oxygen) composition that is made before the gases enter the furnace tube.

Failure Mechanisms

Silicon crystal defects, photolithographic process errors, photo resist or dust contamination, and surface films or stains produce anomalous diffusion effects, as previously described. If stains or films are present on the silicon surface where diffusion is to take place, the diffusant concentration and diffusion depth are affected. This will alter the electrical characteristics of the microcircuit. The other problems may produce latent failures, and, once again, the burden of loss is on the user, for screening of such flaws is a painstaking job with little dividend. It is virtually impossible to visually screen for diffusion faults; diffusion induced anomalies primarily being introduced through faults in some prior operation.

Metallization

Technology

Metal contacts and interconnections are created by first vacuum-evaporating an 0.8 to 1.2 μm (8,000 to 12,000 Å) layer of hyperpure metal(s) on the silicon wafer. Prior to the evaporation, contact windows in the silicon oxide are created by photolithography. If the silicon oxide is not completely removed from the windows during oxide etching, high resistance contact of the evaporated metal to the silicon will result.

The evaporation must take place in a moderately high vacuum $\leqslant 10^{-4}$ N/m^2 ($\leqslant 10^{-6}$ torr) to obtain a reasonably clean film. The surface of the wafer must also be dry and free of stains, film, and dust in order to obtain good adherence of the deposited metal film. Proper distance of the wafer from the evaporant source and location of the wafer with respect to the source is necessary to ensure uniformity of thickness of the evaporated layer(s) and to prevent thinning (shadowing) of the layer over steps in the various oxide diffusion and contact windows. The thickness of the layer(s) is also controlled by the temperature of the source and the time allowed for deposition. Once the metal layer(s) is deposited, the metallized surface within the area of the matrix of circuits on the silicon wafer must not be touched by tweezers or other handling tools.

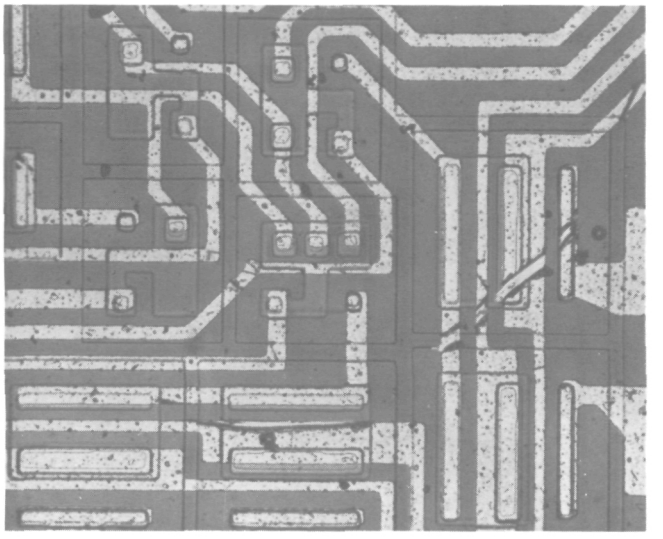
The geometry of the metal contacts and interconnection is produced by the inverse of the photolithographic process used for creating windows in the oxide. The photo resist is placed on the metal layer on the silicon wafer but is exposed to a pattern in which the interconnection design on the glass plate is transparent, rather than opaque (there are positive resists, reverse of the normal, in which normal patterns are used). In developing the resist, all portions are washed away except the exposed pattern. The metal layer is etched and all metal is attacked except the interconnection pattern, which is protected by the photo-resist mask. The resist is stripped and the wafer now has a matrix of circuits complete with contacts and interconnections.

Failure Mechanisms

Problems with metallization often result from either mishandling or flaws in the photolithographic process. Figures 17(a) and (b) demonstrate two problems resulting from mishandling. Rejection criteria will be quite similar to those discussed in "Photolithography." MIL-STD-883 lists the following rejection criteria:

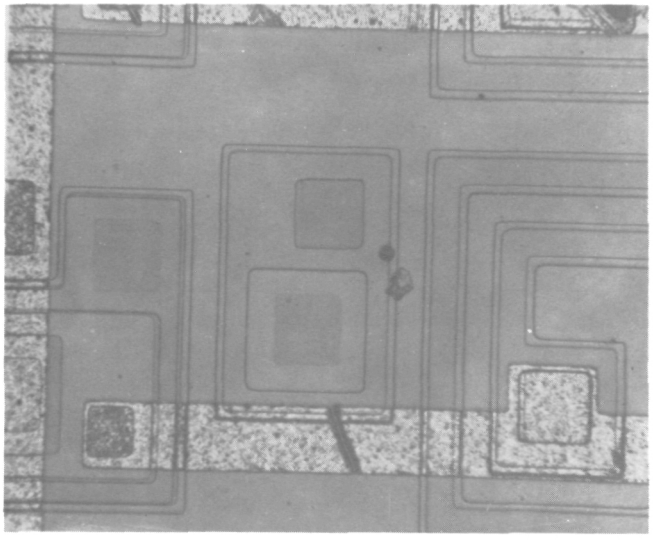
- A scratch or void in the interconnecting metallization which reduces the width of the conducting stripe to less than one-half of the minimum designed width (figures 14 and 17(b)).
- Any scratch or void in the metallization over a contact cut if the defect isolates more than one-half of the designed contact from the interconnecting metallization (figure 13).
- A scratch or void in the bonding pad metallization which isolates one-half of the bond from the metallization stripe (figure 13).
- Any scratch or void at, or over, an oxide step, which reduces the width of the conducting stripe to less than three quarters of the designed width.
- Any device with any evidence of corrosion, or lifting or peeling of the interconnecting metallization (discussed under "Cleanliness").
- Any metallization which bridges two metallized areas such that the distance between those areas is reduced to one-quarter of the designed separation (figures 12 and 13).
- Any device in which the metallization does not cover three-quarters of a designed contact window (figure 16).

If proper control is not exercised during the photolithography, as previously described, inadvertent etching of an interconnection or a contact will take place, or failure to etch a region will occur. The inadvertent etching might result in an interconnection being severely reduced in width over a small distance (as will also happen from handling scratches). Current in the interconnection is, therefore, crowded through a very narrow region and a hot spot is created (figure 14). If the defect is not noted before the package is sealed, the device may later fail as a result of localized heating of the stripe.



(a)

Reject-
Scratch through
metallization



(b)

Reject-
Scratch through
metallization

Figure 17. Scratches in metallization stripe, optical photographs.

On the other hand, if some unwanted portion of the evaporated metal is not etched, there is a possibility of two types of failure mechanisms originating: (a) An unetched metallization path is left between adjacent interconnection stripes, between adjacent contacts, or between an adjacent contact and interconnection stripe. (b) An unetched metallization path is left between adjacent interconnections, but the path begins at one member and terminates very close to the other member, but not touching it.

The first case produces a direct short and is detectable in visual production inspection or electrical tests. The second phenomenon often escapes visual or electrical detection and ends up as a latent failure. The defect is slightly less difficult to screen than some of the other defects described in diffusion, oxidation, and photolithography. It usually reveals itself as an electrical short during low temperature testing, when residual air inside the microcircuit package condenses on the surface of the microcircuit and conductively bridges the gap between the metal path termination and the adjacent metal region.

Another serious problem is a latent electrical "open" due to slow, corrosive disappearance of an interconnection (reference 15). Failure to thoroughly rinse the metal etching solution will leave etching salts deposited along the edge of an interconnection. If any photo resist is left on the interconnection, chemical salts may also be trapped in the resist. In the presence of very small amounts of residual water vapor in the sealed package or water vapor from definite package leaks, the salts react with the aluminum, gradually causing the aluminum to disappear. Since the failure mechanism is time-dependent, another screening enigma arises. Contamination is discussed further in the section on cleanliness.

The most serious problem heretofore encountered with metallization has been related to discontinuities in the metal at the step in the silicon dioxide at a contact window (reference 16). At these points, the oxide has been preferentially removed (etched) so that ohmic contact can be made to the underlying silicon. The causes of the opens are numerous: shadowing, sharp profiles of the oxide steps, undercutting, excessive sintering temperatures, differences in coefficients of thermal expansion, and combinations of the above. The actual discontinuities are usually extremely small, and, therefore, not detectable during visual inspection. Figure 18 is a scanning electron microscope picture of such a fault. Considerable undercutting of the metallization is evident. This problem is aggravated by the fact that the oxide cutout (contact window) was not completely covered by the metal.

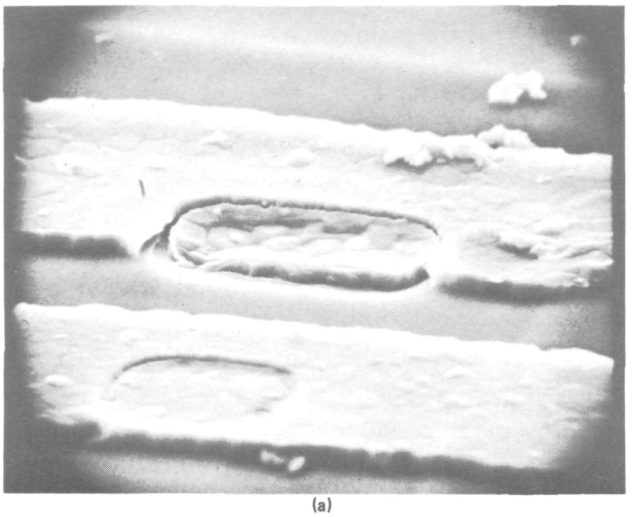
Wafer Probing

Technology

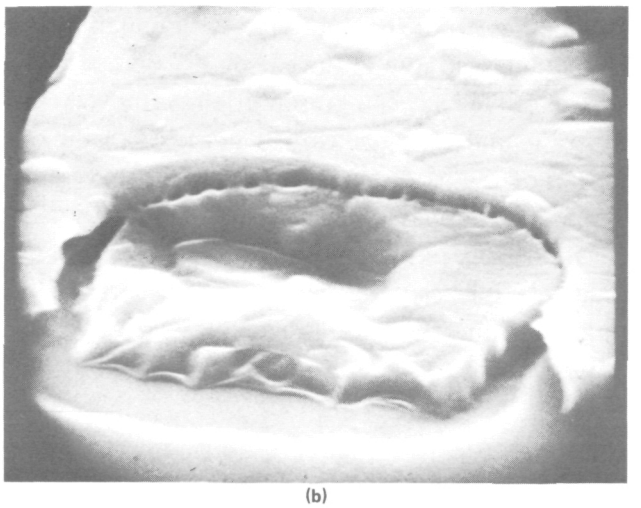
Each circuit of the matrix of the silicon wafer is electrically tested after establishing contact by means of fine pointed, micropositioned probes. These probes are small, approximately 25 μm in diameter, and the connecting wires are attached to automatic testing machines. The actual motion of these probes is mechanically controlled in a vertical (Z-axis) motion which allows the probes to drop down so that they make actual contact with the metallization of the chips.

Failure Mechanisms

This motion of the probes often results in a scrubbing motion which causes scratches in the metallization, particularly in aluminum. Care must also be exercised in positioning the probes as the sharp points may cause scratches of the interconnect metallization (see figures 13 and 17). A detectable short or the origin of a potential conductive path will be



(a)



(b)

Figure 18. Scanning electron microscope photographs of metallization around a contact window. (a) 2100X; (b) 4900X.

created, as was illustrated in the section describing metallization. Aluminum, since it is softer than the metal used in the gold-molybdenum system, is particularly susceptible to scratching, smearing, or other deformation. Handling of the wafer and the microcircuits later on in the fabrication process becomes critical, because tweezers used for holding the parts can produce deformation and serious electrical problems. To prevent such damage, the silicon should be held at the edges with soft tipped tweezers. The damage, unless seen during visual inspection, does not always produce failure in subsequent screening by the manufacturer, and the user is faced with another reliability problem. The failure mechanism is the same as that described for an interconnection wire which has been reduced in width

by the inadvertent etching or photolithographic faults. The rejection criteria are identical to that for scratched and/or etched metallization. The visual inspections are fast, 10 to 15 seconds per circuit, and often subject to operator interpretation. Thus many flaws of this type are passed during the inspection. Many failures in microcircuits delivered to Goddard have been ascribed to such damage.

Wafer Scribing

Technology

Up to this point in the fabrication cycle, all process steps were carried out on full silicon wafers. To complete the cycle, the wafers must be separated into individual chips; this is accomplished in the scribing-and-dicing operation. A weighted diamond stylus is drawn across paths on the silicon wafer separating each device in the matrix. Prior to the actual scribing operation, the oxide on the wafer is preferentially removed along each scribing path so that the diamond point can scribe along bare silicon. Scribing sets up stress patterns in the silicon, and when the wafer is flexed over a sharp edge, the wafer fractures along the scribe lines.

Failure Mechanisms

If the diamond point tears the silicon, small cracks are introduced along the edges of the chips, some of which may point toward the active circuits on the chips. Fine particles of silicon are also given off and redeposited over the surfaces of the chips. The particles are difficult to remove and attempts to remove them often cause scratches in the metallization. Silicon particles are conductive and any remaining on the surface of the chips could produce electrical shorts at a later time. Visual inspection is best for screening this problem; electrical screening is ineffective unless a short occurs.

MIL-STD-883 states: "Any device with a crack on the silicon die that exceeds 1 mil [25 micrometers] in length and points toward an active area, metallization, or bond shall be rejected." Figures 19(a) and (b) list rejection criteria for chips and cracks. Cracks at the edges of the chip may later propagate into the circuit (see figures 19(c) and (d)). Such cracks most probably isolate parts of the circuit, causing catastrophic failure. If a crack propagates in the silicon and underneath an aluminum interconnection, the interconnection may not necessarily be broken by the action. Over some gross cracks the aluminum has actually been seen to stretch, and such circuits have even operated under worst case conditions. An effective screening test for cracks does not exist at this time. The gold interconnections have a distinct screening advantage however, for they are broken when the silicon chip fractures.

Extreme care must also be exercised in order to avoid scratching the metallization with the scribing tool. Depending upon the number of dice on a given wafer, the scribing operation will make up to 100 separate scribing operations on a wafer. Each scribe must be aligned

(X, Y, and rotationally) to avoid the metallized areas. Points of failure would be similar to those demonstrated in figure 17. Figure 13 shows visual inspection criteria for scratches.

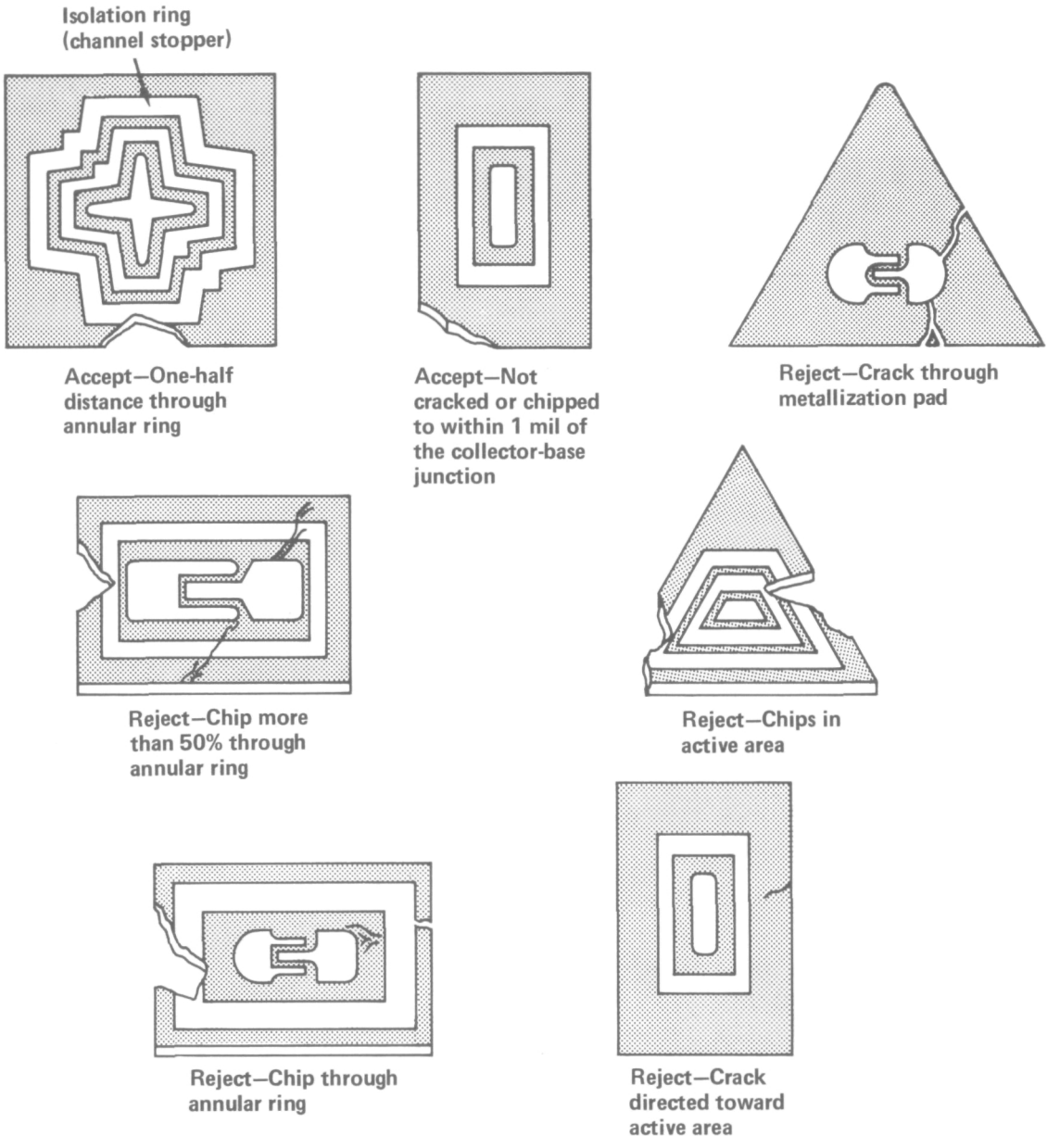


Figure 19(a). Cracks and chips in semiconductor dice, visual inspection criteria.

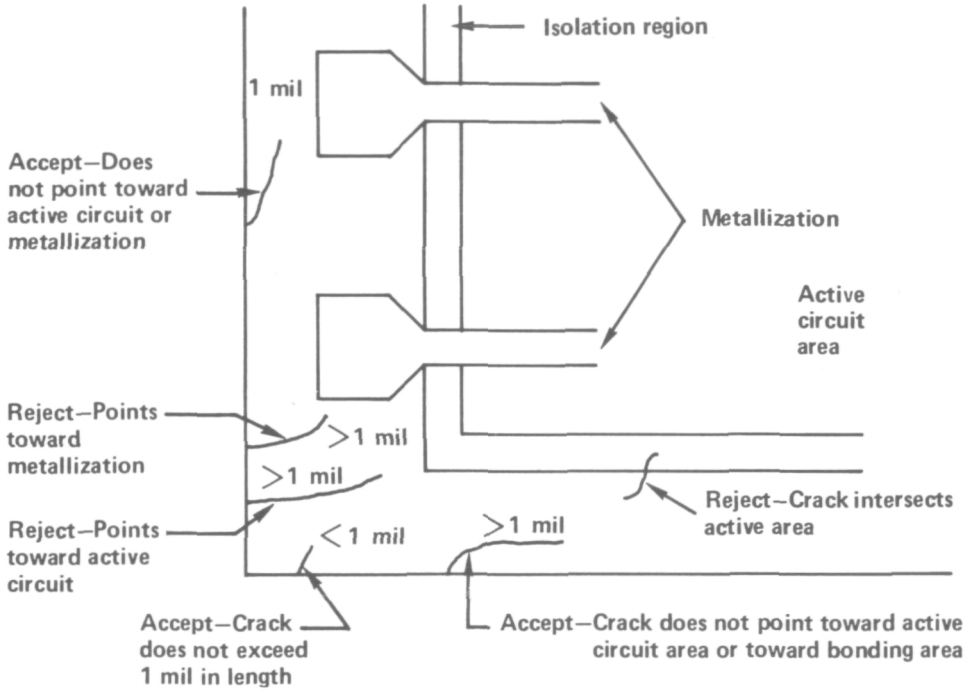
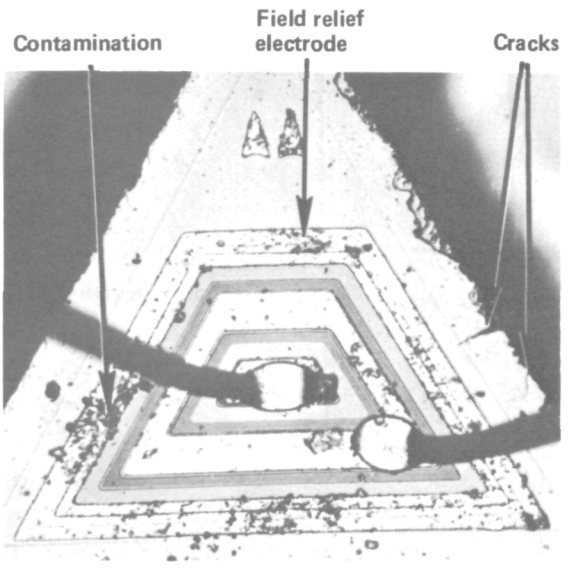
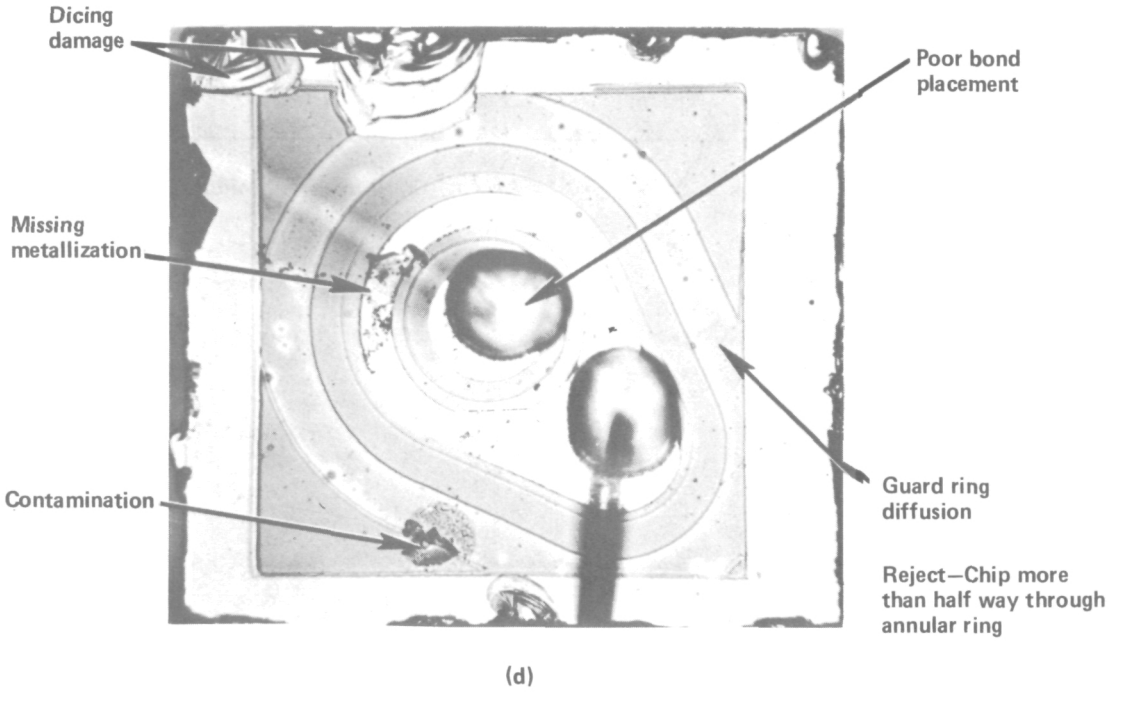


Figure 19(b). Cracks and chips in semiconductor dice, visual inspection criteria.





Figures 19(c) and (d). Cracks and chips in semiconductor dice, optical photographs.

PACKAGING TECHNIQUES

Bonding Of Silicon Chip To Package

Technology

The silicon chip is mounted and bonded to the inside of the bottom half of a package. The package may be either a cylindrical TO type, a flatpack, or a dual-in-line type (larger than a flatpack and with leads bent 90° to the plane of the package). Bonding materials are usually gold-silicon eutectic (with or without preforms), epoxy resin, or Pyroceram glass. (Use of Pyroceram is not recommended for spaceflight use although it is sometimes allowed because of scheduling constraints.) Bonding temperature ranges from 475 to 775 K (200° to 500° C), and bonding times from a few seconds to 5 minutes. Glass bonding is the longest of the operations, and the gold bonding, the shortest.

Failure Mechanisms

In any of these operations, voids may be formed in the bonding material by the outgassing of the parts during the heating cycle. Escape of the gas from the confines of the small flat package or from underneath the silicon chip is difficult, and the gas is ultimately trapped because the bonding material rapidly hardens while cooling. The voids produce uneven stresses in the bonding material and these stresses are, in turn, exerted upon the silicon chip. Mechanical or temperature shock, or the placement of thermocompression bonds at a point over the void, further stress the silicon. The combination of these stresses and uneven void stresses, plus weakening defects in the silicon crystal, may cause the silicon to crack. Figure 20 shows a silicon chip which cracked in this manner.

Additional damage is produced when the operator attempts to seat the silicon chip in the bonding material while the bonding medium is melting or is in the form of a slurry. Vacuum pencils or tweezers used for this purpose are often placed on top of the chip to accomplish the seating, and scratching and smearing of the metallization occur. This problem is again similar in nature to that shown in figures 13 and 17.

Sometimes, despite all precautions, a chip does not bond properly and, as a result, is "cocked" on the header package. This problem can result in the chip becoming dislodged during subsequent use, particularly if such use entails any shock or vibration. This is shown in figure 21. In the course of the visual inspection, particular note should be taken of the amount of bonding material evident around the periphery of the chip. A unit shall be rejected if there is incomplete bonding caused by any of the following (figure 21(b)):

- Less than 75-percent wetting around the periphery of the die
- Bonding material extending over post glass
- Bonding material extending over chip
- Having foreign material under the die holding it off the header
- Having an unmelted preform

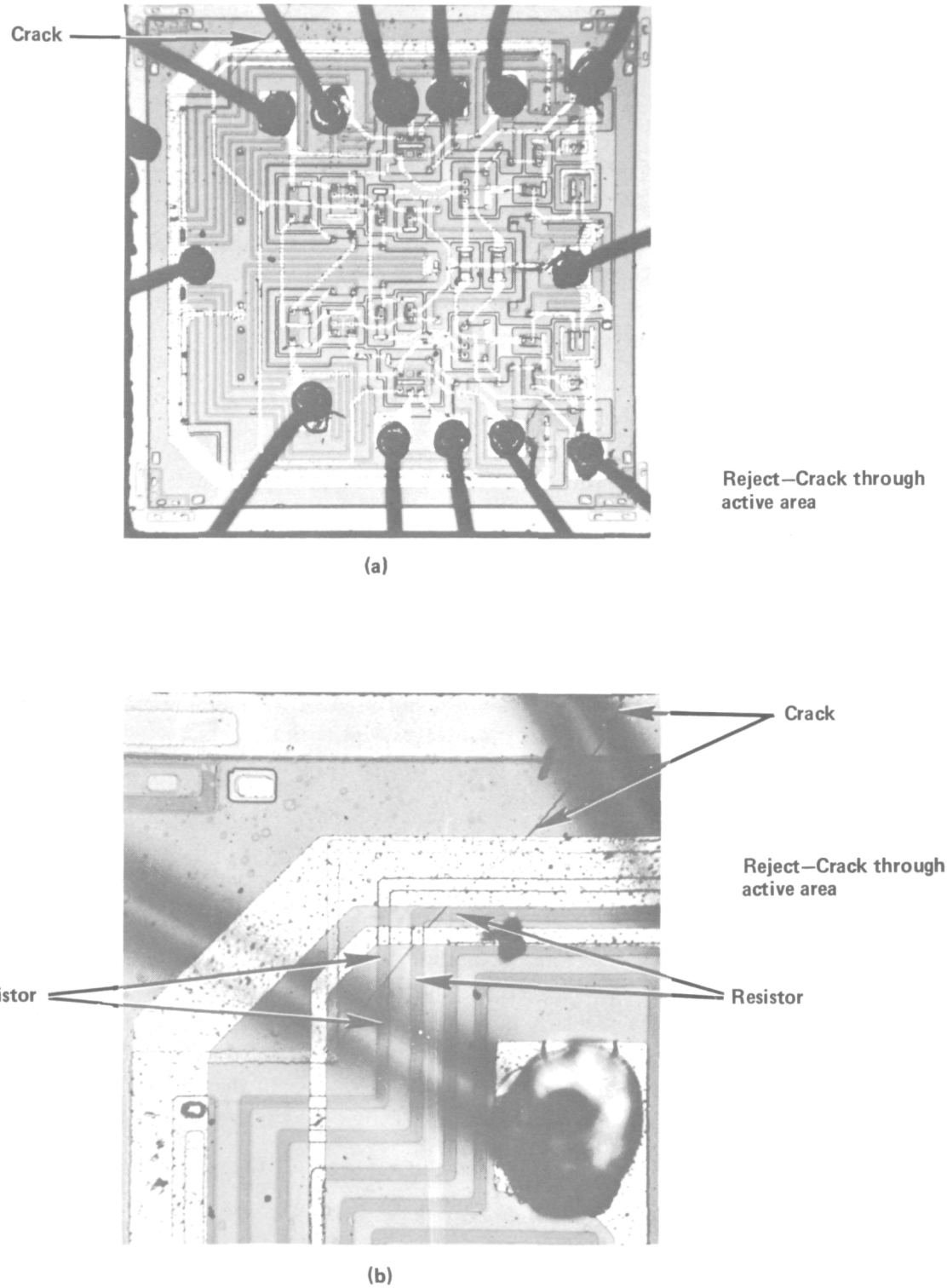


Figure 20. Cracked semiconductor die. (a) 60X magnification; (b) 250X magnification.

Subsequent (post-fabrication) screening is often effective in weeding out these problems. X-ray examination will often detect a cocked or improperly bonded chip, and shock and/or vibration tests are often effective in breaking loose such a chip prior to its intended application.

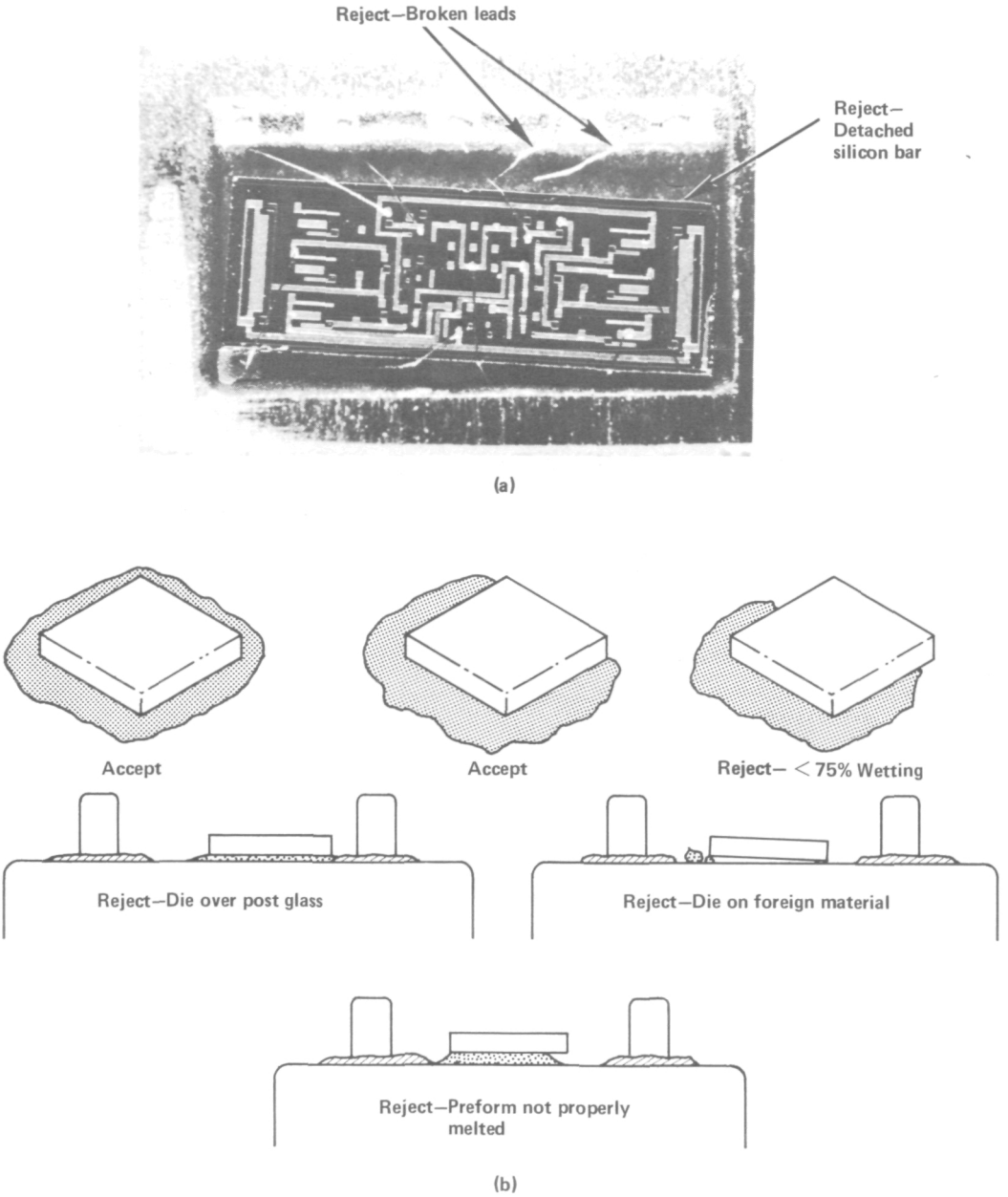


Figure 21. Improperly bonded semiconductor die.
(a) Optical photograph; (b) Visual inspection criteria.

Lead Bonding

Technology

The metal contacts on the silicon chip must be connected to outside circuitry. This is accomplished by bonding fine diameter, 18- to 50-μm (0.7- to 2-cm) long wires to the contacts and to the external leads which come through the package. Three major techniques are usually employed. One process involves bonding wire to a metal contact by means of a very small wedge tool pressed against the wire while it rests on the contact (the substrate is held at approximately 600 K). This is known as thermocompression wedge bonding. The second form of bonding involves the pressure of a capillary tool against a beaded or balled end of a wire while resting the ball on the contact (the substrate is similarly heated). This technique is called ball bonding. The wire is actually fed through the capillary and, as it exits from the capillary, a small portion is melted into a ball by means of a hydrogen flame. The last method, ultrasonic bonding, employs an ultrasonically driven wedge tool which rubs the wire at an ultrasonic frequency while the wire rests on the contact (no heat is necessary). Drawings of these three types of bonds are shown in figure 22. Wedge and ball bonds commonly employ gold wire, while ultrasonic bonding is best accomplished with aluminum wire. In most cases the bonds are made on aluminum contacts, although gold-wire ball bonds to gold contacts over molybdenum are becoming popular.

The other ends of the wires are terminated on the ends of the external leads which come through the package. Bonding is effected by pressure of the bonding tool against the wire where it rests on the external lead. The wire is either cut or melted to separate it from the bonding instrument. The metal system involving these bonds and the lead posts is usually monometallic, and intermetallic-formation problems are avoided. The external leads are Kovar metal (an alloy of nickel, cobalt, and iron) and are gold plated external to the package and either gold plated or aluminum plated inside the package. Figure 23 is an exploded view of the flat package showing internal wire leads. Figures 24(a) through (d) are a series of scanning microscope photographs of typical bonds.

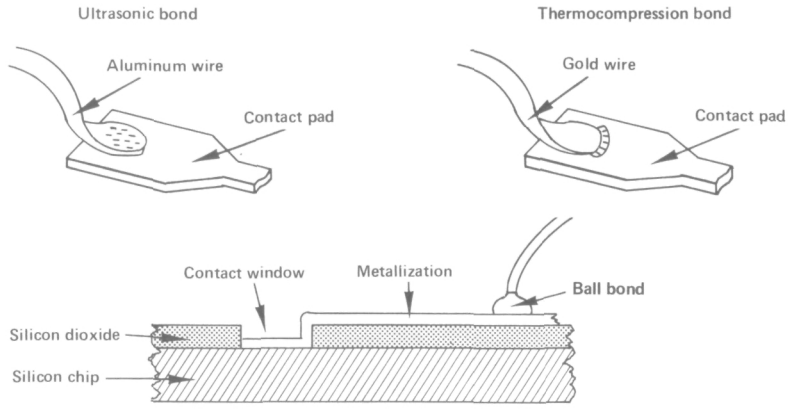


Figure 22. Typical package materials and connections for flat package type encapsulated microelectronic circuits.

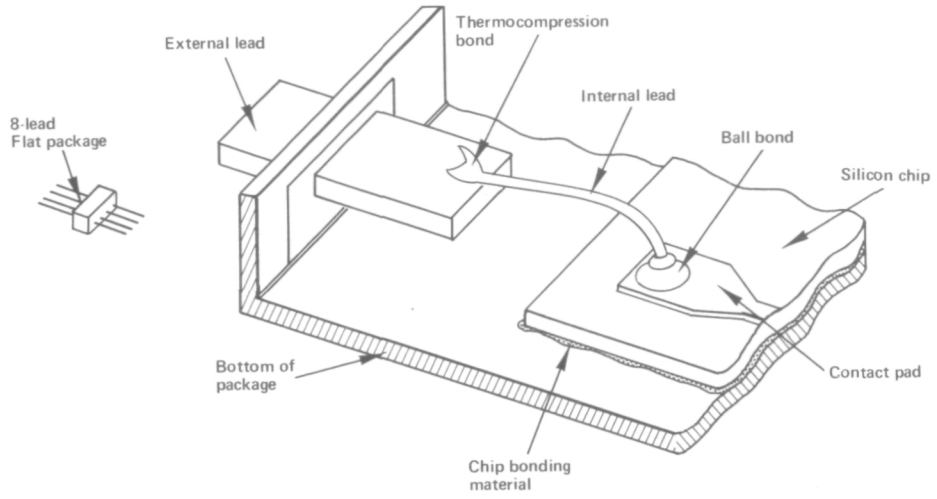


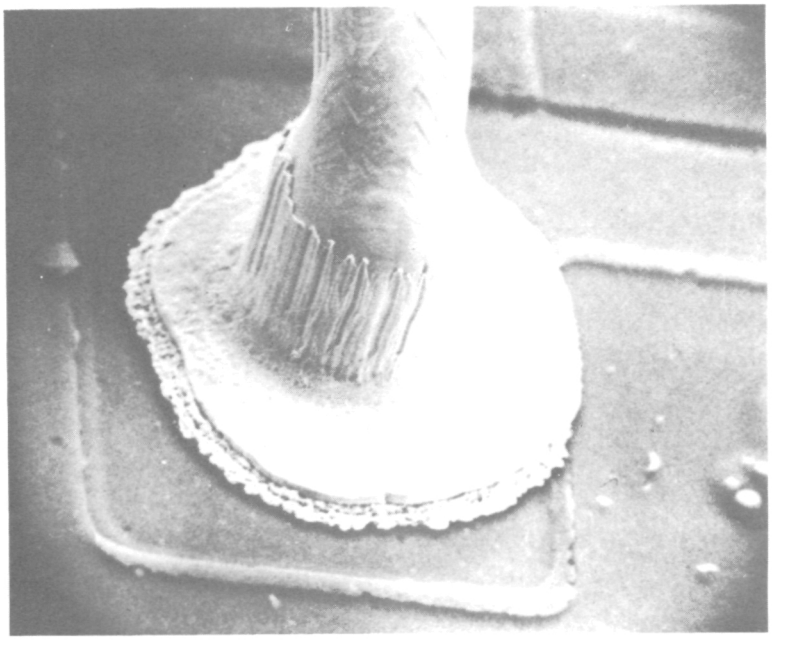
Figure 23. Exploded view of internal section of flat package.

Failure Mechanisms

Actual rejection criteria, as per MIL-STD-883, are as follows:

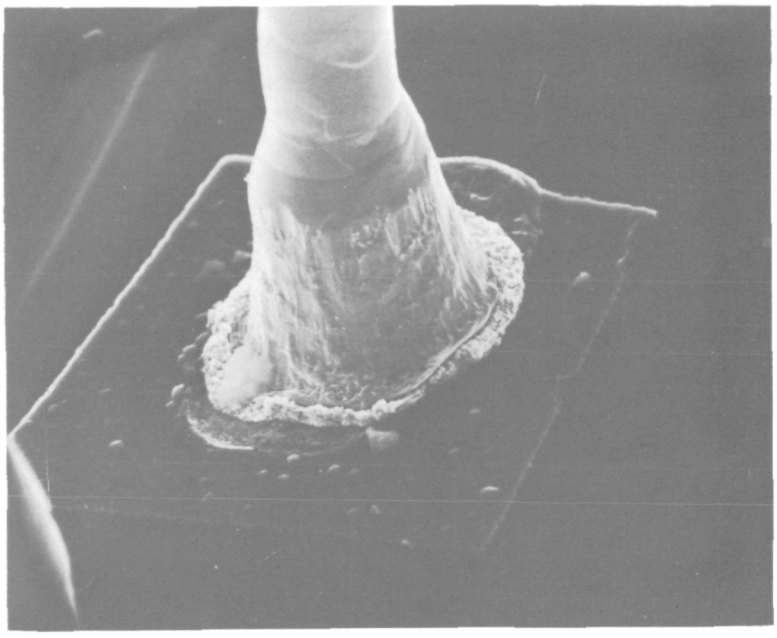
- Wire loops greater than 3 times the bonding wire diameter (figures 25(a), (b), and (c))
- Devices with bonds placed so that the wire from the bond passes over another metal bonding pad (figure 25(d))
- Nicks, cuts, crimps, or scoring of the bonding wire which reduces the wire diameter by 25 percent
- Neck-down of the bonding wire caused by excessive lead tension which reduces the diameter by 25 percent
- Extra lead wires or pigtails of more than 75 μm (3.0 mils) in length
- Any device with ball bonds to the semiconductor chip which are less than 2 times or greater than 6 times the diameter of the bonding wire
- Ultrasonic bonds to the semiconductor chip that are less than 1.2 times or more than 3.0 times the diameter of the wire
- Devices with bonds placed on bonding pads such that less than 50 percent of the bond is within the bonding pad area (figures 26(a) and 27)
- Devices with bonds placed so that the separation between bonds or between a bond and adjacent metallization is less than 13 μm (0.5 mil) (figures 26(b) and 27)

(a)

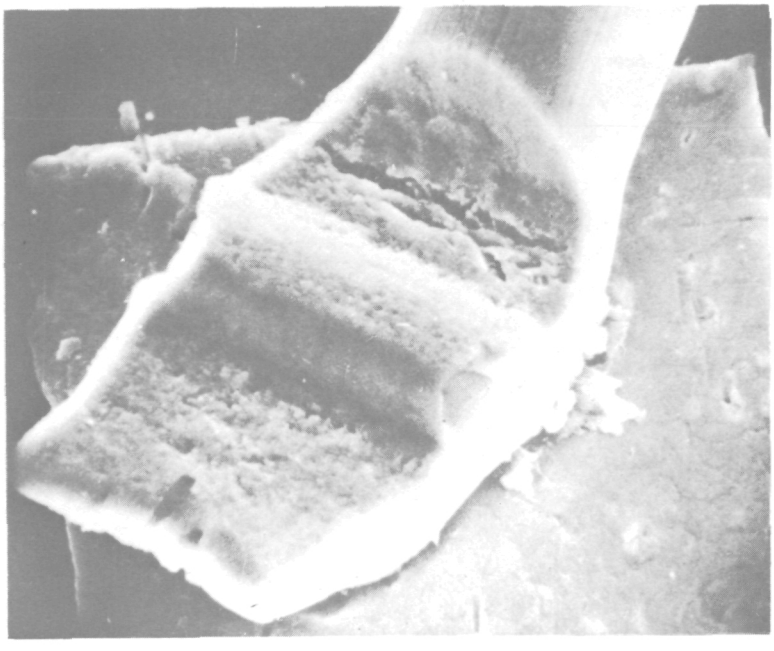


(b)

Figure 24. Scanning electron microscope photographs of typical wire bonds. (a) Proper gold ball bond (but considerable intermetallic formation is present); (b) Overbonded gold ball bond.

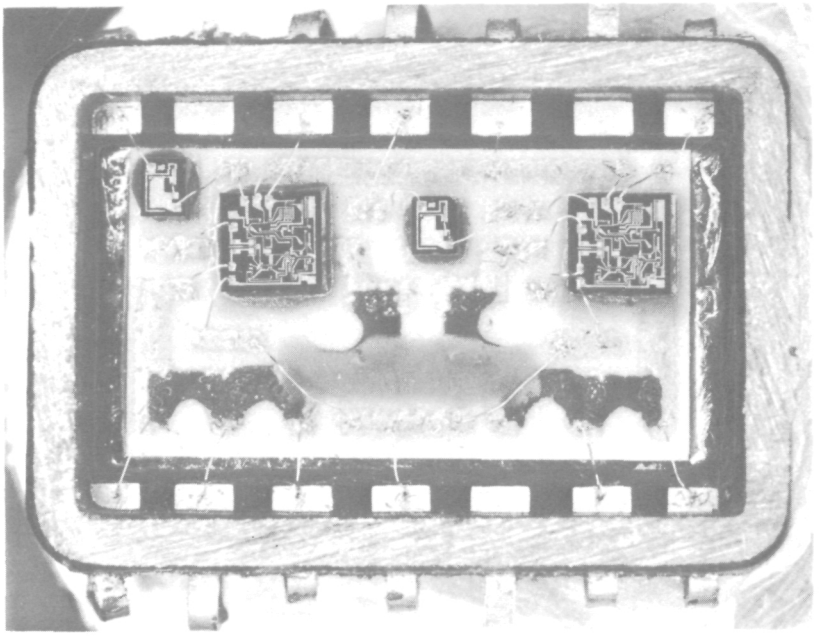


(c)



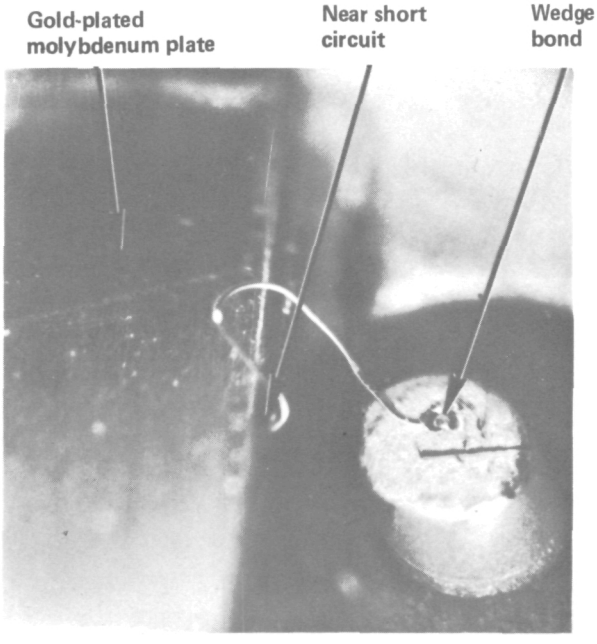
(d)

Figure 24. Scanning electron microscope photographs of typical wire bonds. (c) Ball-less gold ball bond; (d) Aluminum ultrasonic bond.



Reject—Loop more
than 7 wire diameters

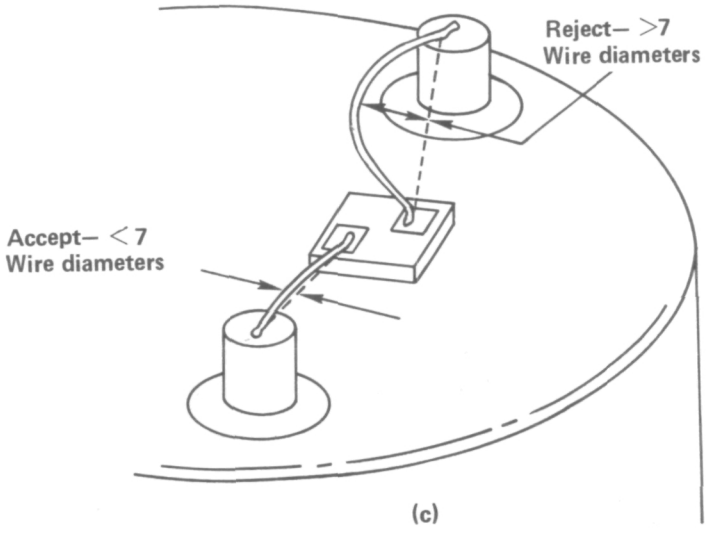
(a)



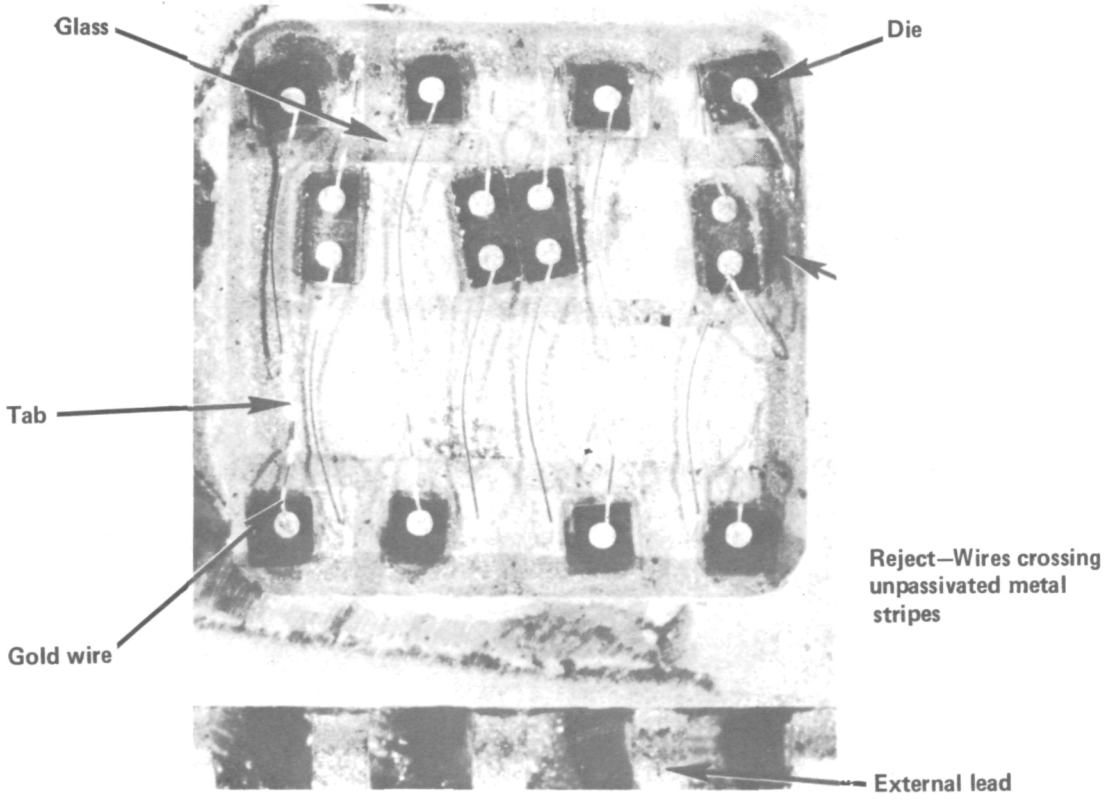
Reject—Loop more
than 7 wire diameters

(b)

Figure 25. Problems associated with wire leads.
(a) Excessive wire length; (b) Excessive wire length.



(c)



(d)

Figure 25. Problems associated with wire leads.
(c) Visual inspection criteria; (d) Wire leads crossing conducting path.

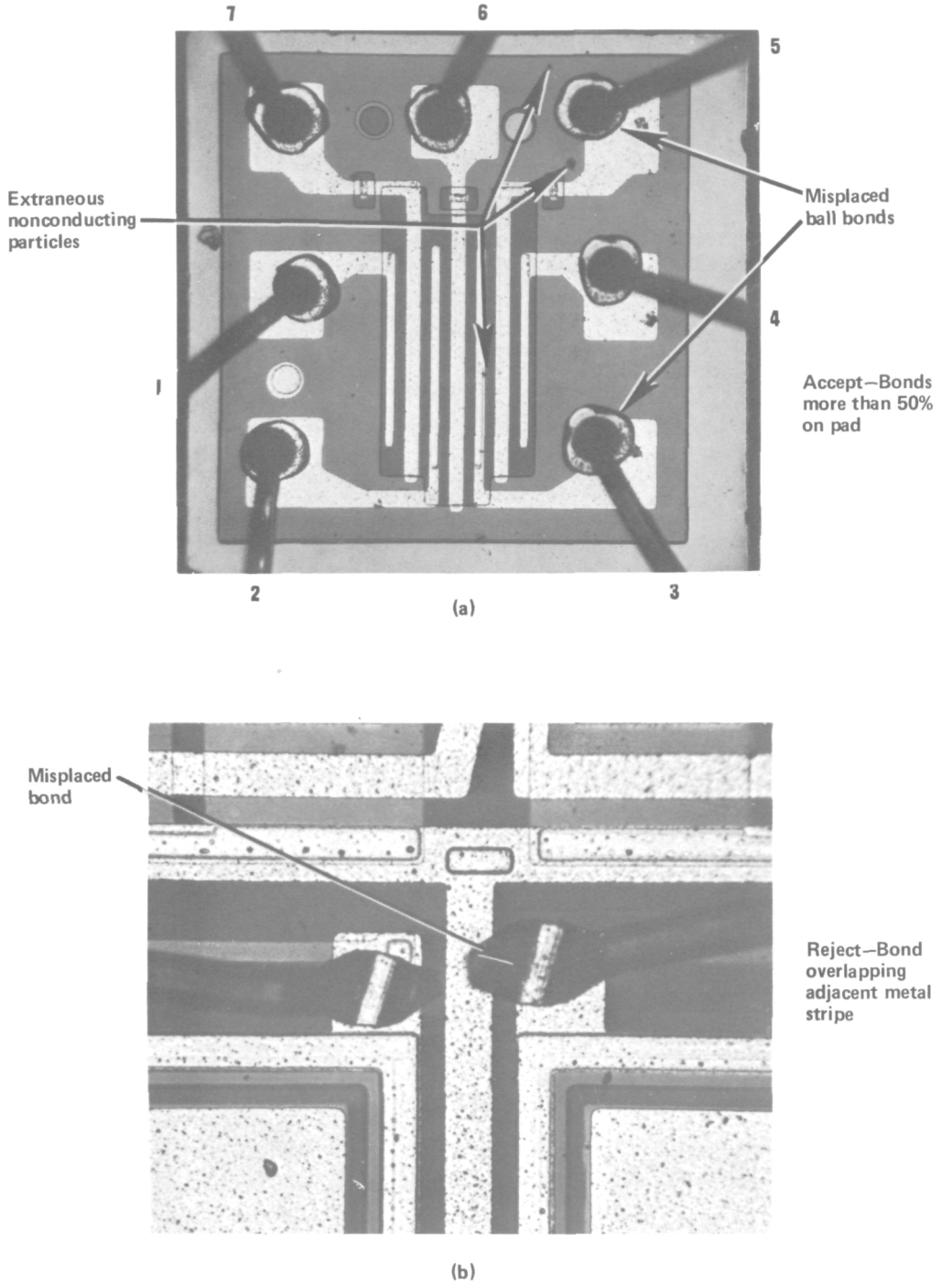


Figure 26. Representative wire bonds.
(a) Misplaced ball bonds; (b) Improper bond spacing.

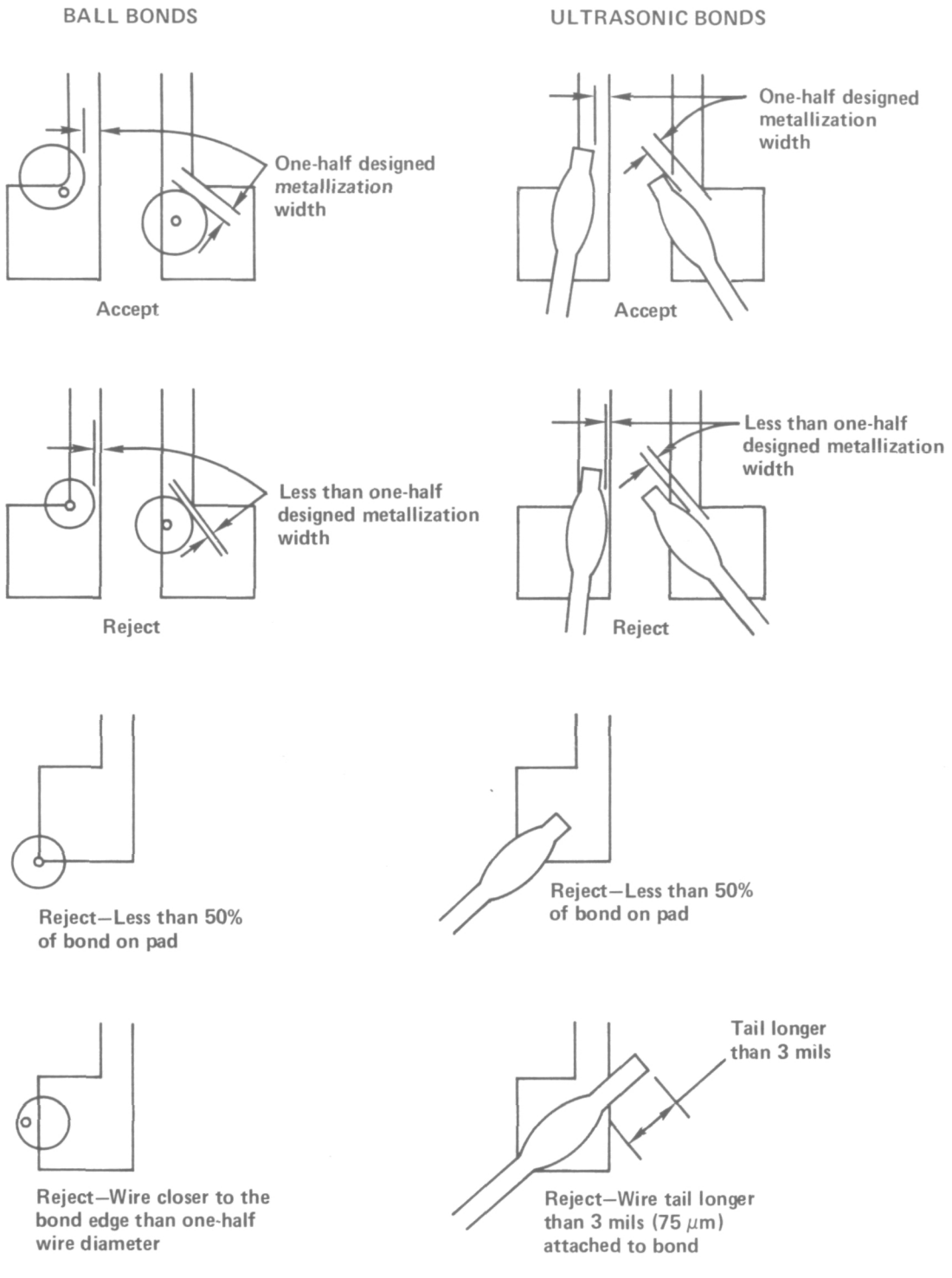
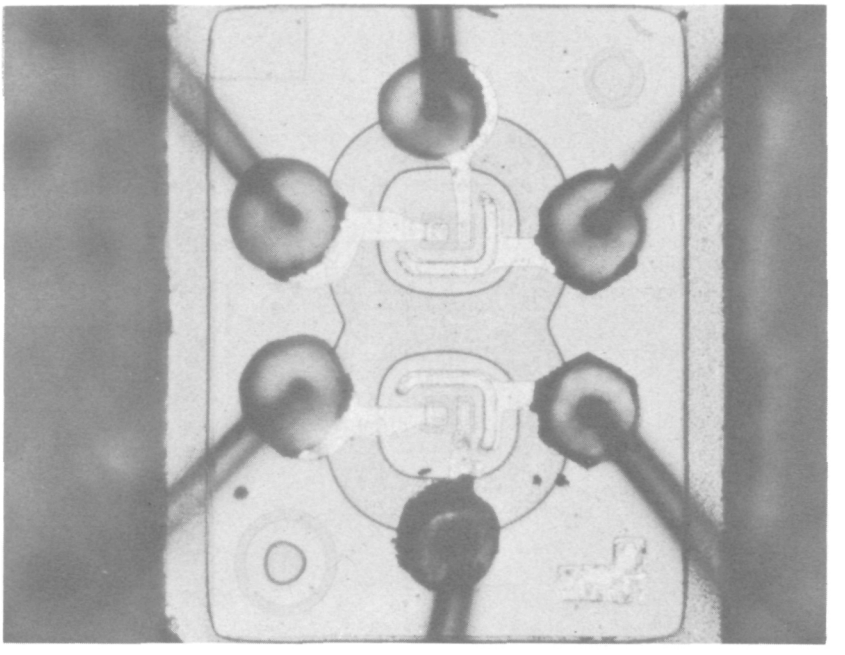


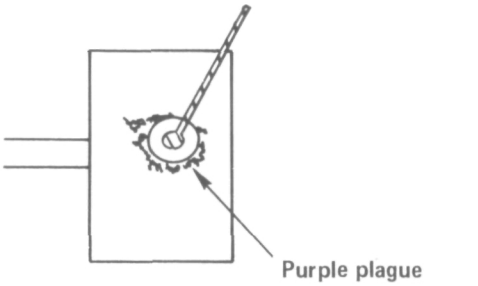
Figure 27. Representative wire bonds, visual inspection criteria.

A major drawback exists with gold to aluminum or bimetallic bonds in that (a) the existence of intermetallic phases (often referred to as purple plague) within the bonds initiate bond cracks, and (b) mass transfer (Kirkendall Effect) of the metal(s) produces microvoids in the bond (references 16, 17, and 18). If the silicon is overheated during bonding of a gold wire to aluminum, or if the sealed device is stored in temperatures of 475 K (200° C) or higher, intermetallic phase formation is accelerated, and the device will have a limited operational life (figure 28). There is no absolute satisfactory way to screen for bonds with intermetallic



Reject—Excessive intermetallic phase

(a)



(b)

Figure 28. Intermetallic phase formation.
(a) Optical photograph; (b) Visual inspection criteria.

faults, since it is a time- and temperature-dependent phenomena. Visual inspection should reject those bonds which are distorted or cracked due to the use of too high a bonding pressure and/or temperature (overbonding) (figure 24(b)). On the other hand, there is the underbond, where insufficient heat and bonding-tool pressure are employed and the bond is just tacked on. The bond is difficult to judge by visual inspection, and mechanical shock or vibration screening would have to be performed to work the bond loose. Sample pull testing of bonded wires is another screening method. In sealed units, electrical tests made at very low currents (threshold tests) between various pin combinations can sometimes detect faulty bonds. If the bonds are weak enough, mechanical shock or temperature cycling will tend to open them.

Wedge bonds of gold to aluminum are not particularly recommended, since not only may the intermetallic phases weaken the bond, but the thinning of the wire from the wedge tool may induce additional weakening. Bonding pressure and temperature are, therefore, very critical in this operation. Monometallic systems such as gold wire to gold contacts and aluminum wire to aluminum contacts do not experience intermetallic formation and should be more reliable.

Other bond defects are created when the aluminum metallization contact is too thin and is completely drawn into the gold during bonding alloying. The actual failure here is a clean lifting of the bond from the silicon oxide, and an electrical open is created. This failure mode is readily discernible at the factory by visual inspection only if the bond has separated, or by electrical testing after mechanical shock.

Problems are also incurred if the wire length between the bond at the contact and the bond at the external lead is too long. The wire could eventually sag and touch the silicon chip, producing an electrical short at that point, or could short to the lid after the lid was attached. Visual inspection should easily screen the condition (figures 25(a) and (b)). If wires cross one another, or cross other conducting paths, there is also the danger of intermittent shorting. Screening procedures follow the same line as employed for lengthy wires. Figure 25(c) shows cases where wires cross a conducting area.

Some bond discrepancies at the contacts on the silicon chip are noteworthy as they may lead to latent failure. Figure 26 demonstrates a number of examples of bond discrepancies; figure 27 lists the rejection criteria from the referenced Marshall specification. Such improprieties as improper location of a bond on a contact (figure 26(a)) and bonds placed too close to one another (figure 26(b)) can best be seen during visual inspection. Later screening is difficult. Very close proximity of neighboring contact bonds leaves only a very short insulating silicon oxide path between them and, as noted for metallization and scratch defects, a conductive path could easily be created by low temperature condensation. In the latter defect, if only a small portion of the wire is bonded to the contact, the bond will be weakened. A number of subsequent mechanical shocks or vibrations may cause the bond to open.

As circuit complexity increases, the possibility of operator error in bond positioning also increases; that is, a bond may be made to an incorrect bonding pad (figures 29(a) and (b)). This situation is extremely difficult to observe, unless the individual performing the visual inspection has more than a casual familiarity with the circuit layout. In other words, the visual inspector must be prepared not only to weed-out the improperly fabricated parts, but must be prepared to notice errors of omission or commission. Bonds of this nature usually would be removed during electrical screening because of the anomalous electrical characteristic(s) resulting from erroneous bond placement. Unfortunately, this is not always the case and parts have been received for failure analysis which had erroneously placed bonds but which, because of some gap in the electrical testing, had passed electrical screening.

Cleanliness

Technology

During the course of the fabrication cycle, there are innumerable instances where the wafers undergo cleaning operations. These procedures are similar to those described above in the section on silicon slicing and polishing; that is, all chemicals should be of the utmost purity, and inspection procedures should be such as to verify that the wafers are indeed clean after the cleaning operation.

However, foreign material is present not only because of an operator's failure to properly remove it—it is often present because of an operator's failure to keep it out. The fabrication of semiconductor devices demands an environment that facilitates the "keeping out of foreign material." Most companies have facilities which are extremely clean (clean rooms) and, in addition, use laminar flow hoods in areas of ultimate criticality; for example, photolithography, final preseal visual inspection, and so on.

Failure Mechanisms

Failure to remove unwanted material from the wafer can cause many problems during the fabrication cycles, as was described above for various steps. Foreign material introduced into the device package from external sources (for example, chemical contamination, particulate material, and such) can cause a myriad of problems. Chemical contamination, while most often arising because of improper cleaning of residues during prior cleaning operations, can result from such sources as dandruff, salt from an operator's skin, and chemical vapors from epoxies or other sources. These contaminants can lead to electrical shorts, device degradation, or metallization removal (etching). MIL-STD-883 rejection criteria are: "Unattached metallic, abrasive or conductive material on the surface of the die or within the package shall not be acceptable. Attached metallic or conductive material shall not be acceptable on the surface of the die if silicon oxide is not visible between the particle and any adjacent metallization.....Conductive foreign material is defined as any opaque substance." Figure 30 demonstrates two examples of chemical contamination. In neither of these cases has the contamination resulted in failure, but, because of the latent nature of

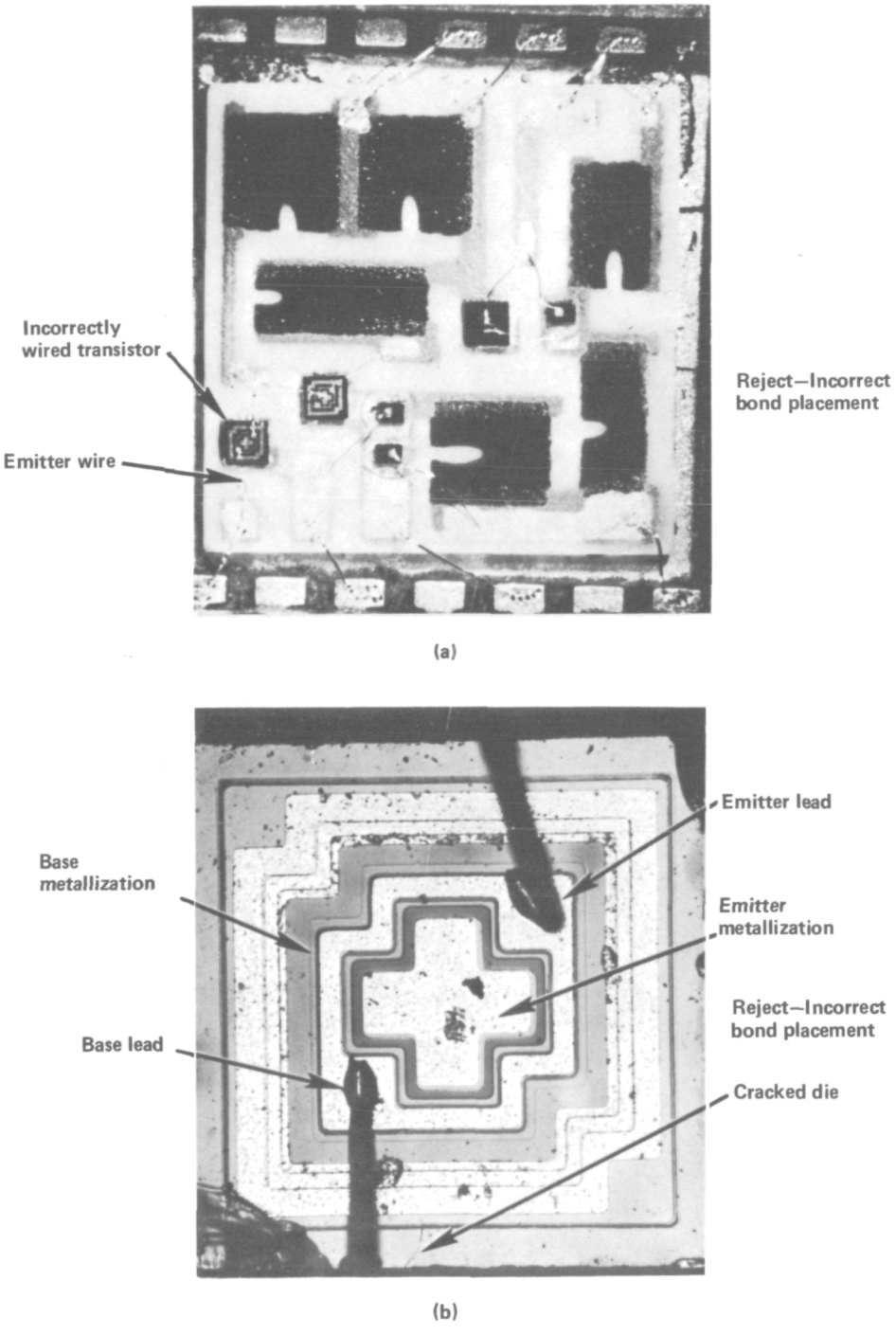


Figure 29. Representative wire bonds.
(a) Improper bond placement; (b) Improper bond placement, higher magnification.

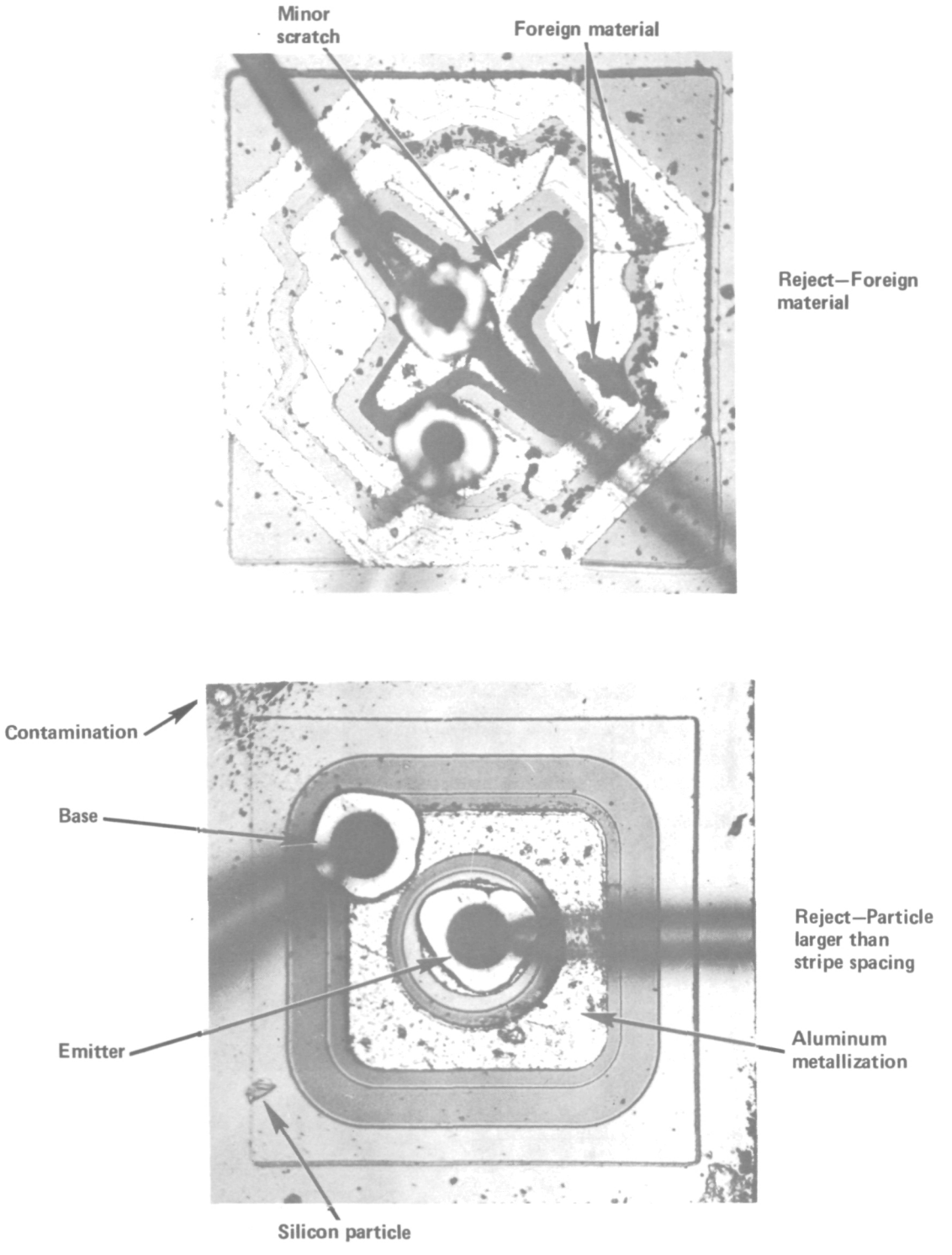


Figure 30. Surface contamination on semiconductor surface.

such problems, neither sample could be accepted. Particulate contamination can arise from a number of sources. Metallic particles can result either from bonding material which improperly wet the device or header surface, or from pieces of cutoff bonding wire, and such. Nonmetallic particles can result from chips breaking off of improperly fractured silicon chips or from pieces of lint introduced from the environment. Figure 31 shows two examples of this type of contamination: figure 31(a) is a case where the particle caused intermittent failure, while figure 31(b) is a case where the particle fused between the metallization stripes, causing catastrophic failure.

Final Preseal Visual Inspection

Technology

The final preseal visual inspection is the last opportunity to visually examine the devices prior to sealing on their lids. This inspection step should be carried out in a dust-free environment; for example, in a laminar flow hood. It is usually performed using an optical microscope with a magnification range of 40X to 400X. Initially, the inspector views the devices at the lowest magnification and changes to higher magnifications whenever viewing critical areas or suspected anomalies. The inspector must be aware of:

- All the potential problems introduced by the prior operations
- The manner in which these problems are visible, if at all
- The seriousness of these anomalies

If the inspector is aware of these items and, if the manufacturing company's philosophy is to produce highly reliable devices, many potential problems can be screened out here. However, if the inspector is poorly trained, and/or the company is not properly motivated, the final preseal visual inspection is of little value. This is true both for integrated circuits and for the more complex hybrid microcircuits, discussed next.

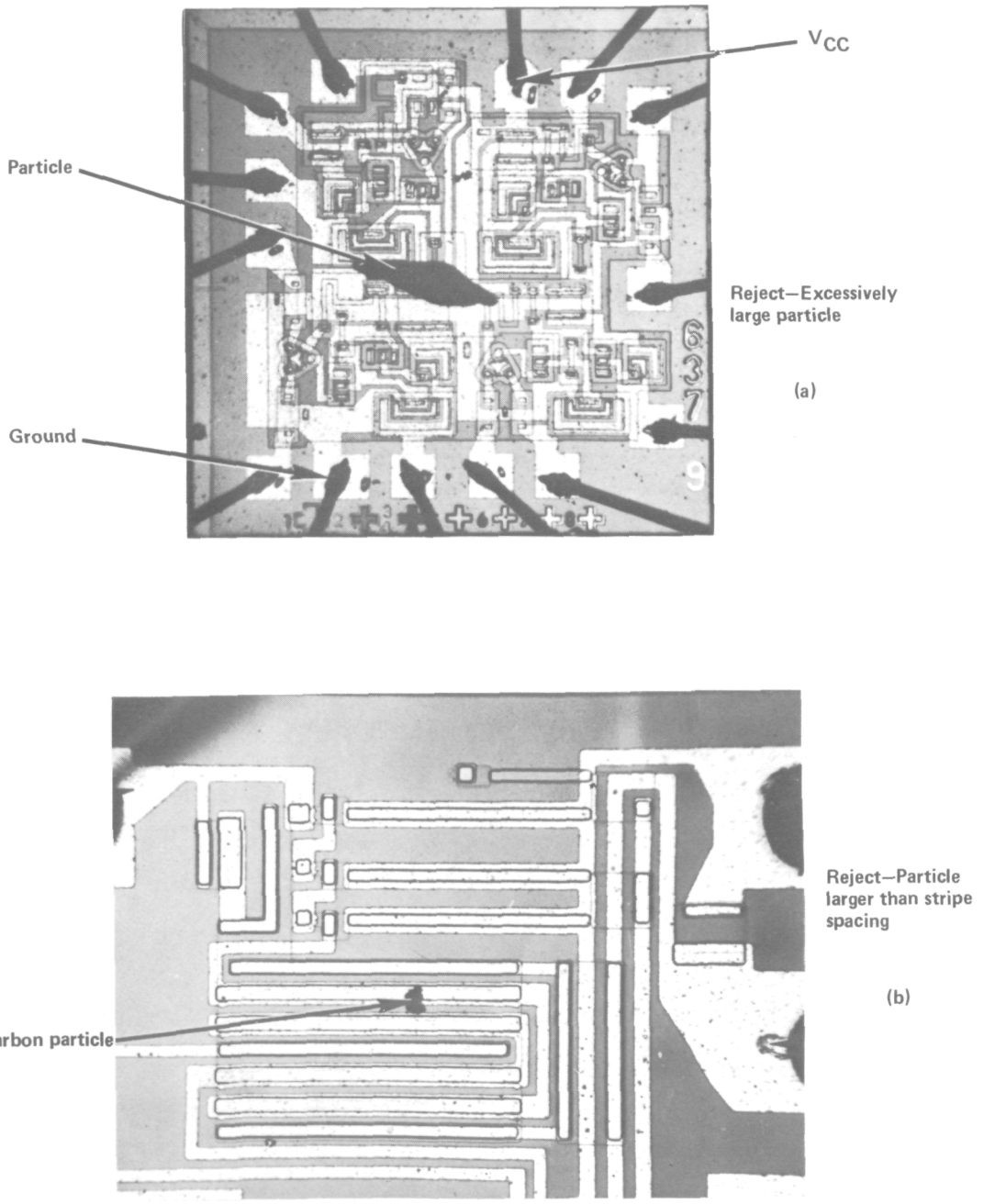


Figure 31. Particulate surface contamination on semiconductor surface.

HYBRID MICROCIRCUITS

In recent years, the use of hybrid microcircuits in space applications has been increasing steadily. The reasons are several:

- For specialized circuits (for example, less than 20,000 to 1,000,000 demand), it is prohibitively expensive to make integrated circuits. Therefore, if it is desired to minimize the space (volume) requirement of discrete devices, hybrids are the logical alternative.
- Some circuits, because of the size of some components (for example, extremely large resistors or capacitors), cannot be fabricated in conventional integrated circuits. They can, however, be constructed by a marriage of integrated circuits, transistors, thick or thin film resistors, and discrete capacitors (that is, hybrid circuits).

The use of these hybrid systems introduces some additional problems that, hopefully, should be screened out at the final preseal visual inspection. Since most of the parts used in hybrid systems are semiconductor devices, the discussion of problems attendant to those devices will not be repeated. Only those failure mechanisms introduced by the additional processing are covered here. To demonstrate the complexity of these circuits, figures 32 and 33 show conventional types of hybrid circuits; figure 32, a thin film circuit; and figure 33, a thick film hybrid circuit.

PREPACKAGING AND PACKAGING TECHNIQUES

Resistor Fabrication

Technology

Several techniques are in use to form the resistors in a hybrid assembly (diffused resistors in silicon substrates are not considered here). Among the more common materials are nichrome, tantalum oxide, and cermets. Nichrome films are deposited using standard evaporation techniques from a source consisting of 80 percent nickel and 20 percent chromium. Tantalum resistors are slightly more complicated; pure tantalum is sputtered onto the substrate and then anodized so that the surface of the tantalum is converted to tantalum oxide (an insulator). This reduces the thickness of the conducting film and adjusts the resistor value. Both types of resistors, nichrome and tantalum, are then etched using photolithographic techniques to form the actual resistor networks. Cermet resistors, a mixture of ceramic and metal, are either evaporated or silk screened onto the substrate. In the silk screen process, a fine mesh screen, either silk or stainless steel, is preferentially blocked out so that openings occur only at predetermined areas and in predesigned geometries. This screen is placed in intimate contact with the substrate and the cermet material, mixed with

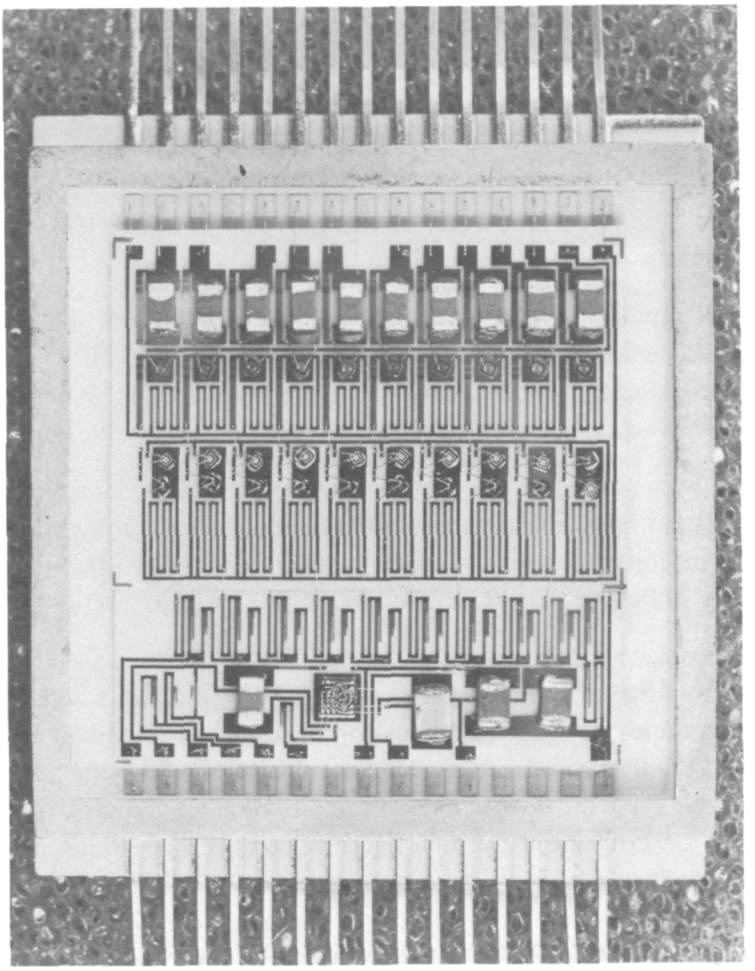


Figure 32. Thin film hybrid microcircuit.

a suitable binder, and squeegeed through the openings onto the substrate. The substrate is then fixed at a temperature sufficiently high to evaporate the binder. These resistors are trimmed (adjusted) either by abrading the resistor with some method such as sandblasting or scribing it with a diamond scribe.

Other types of resistors are used in hybrid assemblies, for example, palladium-silver and tin oxide. The techniques used for their deposition are similar to those described above.

Failure Mechanisms

As in any evaporation or sputtering process, there are many ways in which problems can be introduced into an end product. However, these would ordinarily be manifested as electrical rather than visual problems. A common imperfection in these passive devices which can be seen in a visual inspection is related to the photolithographic step, and the acceptance criteria are identical to those described for integrated circuits. In the cermet

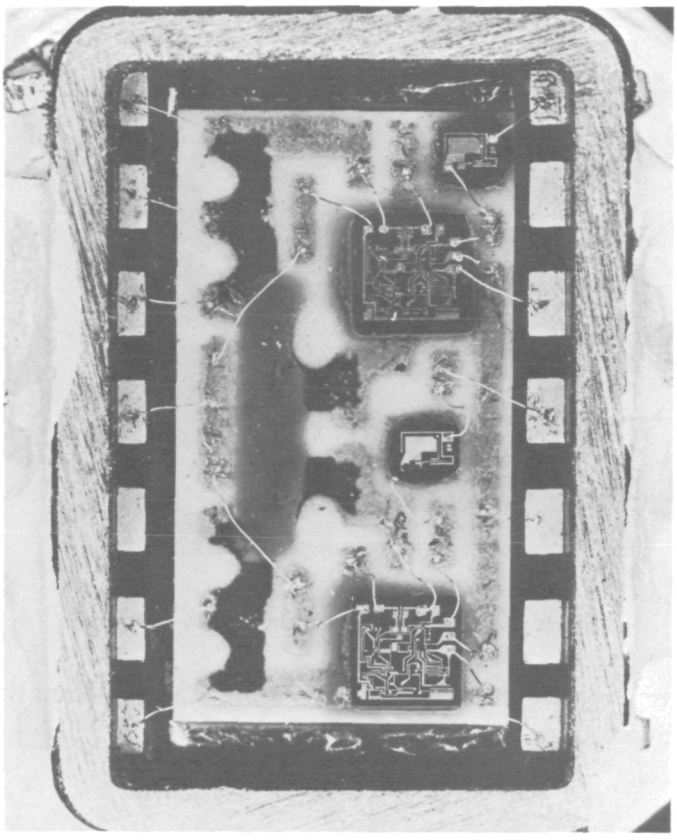


Figure 33. Thick film hybrid microcircuit.

resistors, the scribing operation (trimming) may introduce strains or cracks into the cermet itself or into the substrate. Figure 34 shows a crack introduced by this method.

These resistor elements are extremely thin and therefore quite susceptible to the effects of contamination. The primary effect of this contamination is corrosion or oxidation. Therefore, the presence of any extraneous foreign material is to be avoided.

Capacitors

Technology

Several different types of capacitors are used in hybrid assemblies. These included SiO_2, ceramic, and dry tantalum. The SiO_2 capacitors are not as generally used because of the probability of obtaining pinholes in the large areas necessary to obtain large capacitors. They are constructed by thermally growing a thin SiO_2 layer 100 to 300μm (1,000 to 3,000 Å) on a silicon slice, evaporating a metal film onto the SiO_2 layer, and making contact to the silicon chip and the metal film. The silicon is bonded either with a gold eutectic solder or a conducting paste. Contact to the film is made with wire bonds. Both

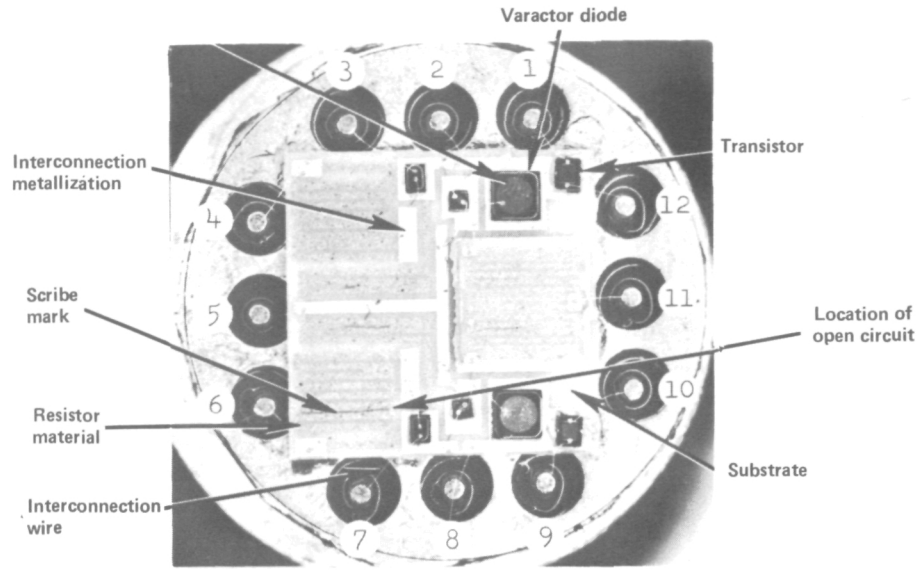


Figure 34. Cermet resistor, trimmed by scribing.

ceramic and tantalum capacitors are purchased as completed chips and their actual construction is not of interest here.

Failure Mechanisms

The most common failure mechanism of the SiO_2 capacitors is concerned with pinholes in the oxide. These, however, are extremely small and masked by the metal film. Failure mechanisms more readily detected visually in any of the capacitor types are related to bonding. The wire bonding would be identical to what occurs in the conventional integrated circuits. The chip bonding, as in conventional monolithic circuits, has caused a number of problems and is covered below.

Chip Bonding (Semiconductor or Capacitor)

Technology

The actual chips used in hybrid assemblies, whether semiconductor devices, capacitors, or ceramic substrates, are bonded either to metallized bands on the ceramic substrate or to the package header. This is effected by the use of silicon-gold alloys, lead-tin solder, or conducting pastes. The silicon-gold solder is primarily used to bond semiconductor chips, while the lead-tin solder or the paste is used to bond capacitors. All three have been used to bond ceramic substrates to the header.

Failure Mechanisms

Fewer problems have been noted with the silicon-gold alloy method of bonding than experienced with the lead-tin solder or the epoxies. The mechanisms most commonly experienced are related either to a lack of mechanical integrity of the bond or to conducting particles. In the first case, the problem arises from a number of causes: improper metallization of the ceramic, incorrect soldering techniques, or lack of manufacturing controls. Occasionally, there are chips which have completely or partially broken loose from their substrate and they are similar to that shown in figure 21. To try and screen out these problems which are often latent in nature, the bonded chips or substrates should be checked for fileting, or at least for complete bonding material around the periphery of the substrate. Fileting, shown in figure 35, can only occur on semiconductors or capacitors since it demands a type of alloying. The rejection criteria listed in figure 21(b) are also applicable here.

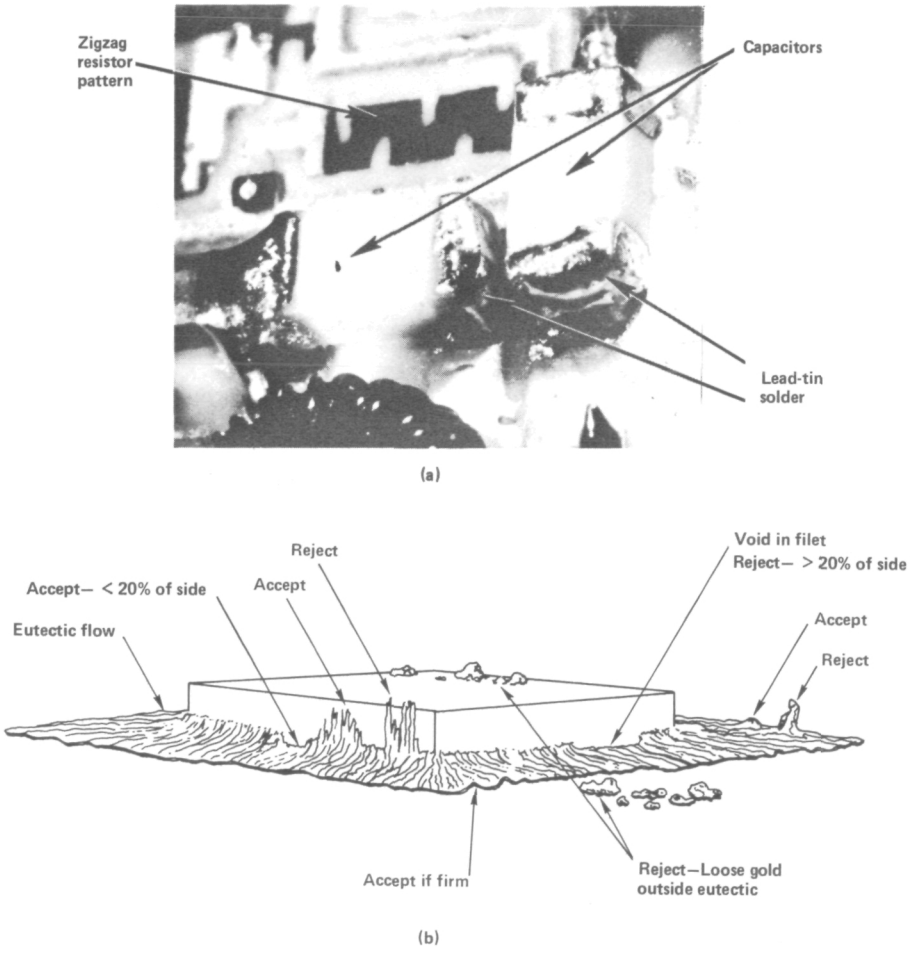


Figure 35. Solder fileting around capacitors on hybrid microcircuit.
(a) Optical photograph; (b) Visual inspection criteria.

Particles are an extremely serious problem in hybrid circuits. Particles occur as a result of improper bonding, scratches in metallization, and so on. If the particles are electrically conducting, they are a great reliability risk; however, even nonconducting particles can cause failures if, during shock or vibrations, they strike a wire bond. Therefore, there should be no apparent particles in the hybrid circuit, nor should there be metallic globules at any of the bonding areas which are attached by a section which is less than one-half the area of the globule (figures 36 and 37). The same rejection criteria described in the section on cleanliness apply here also.

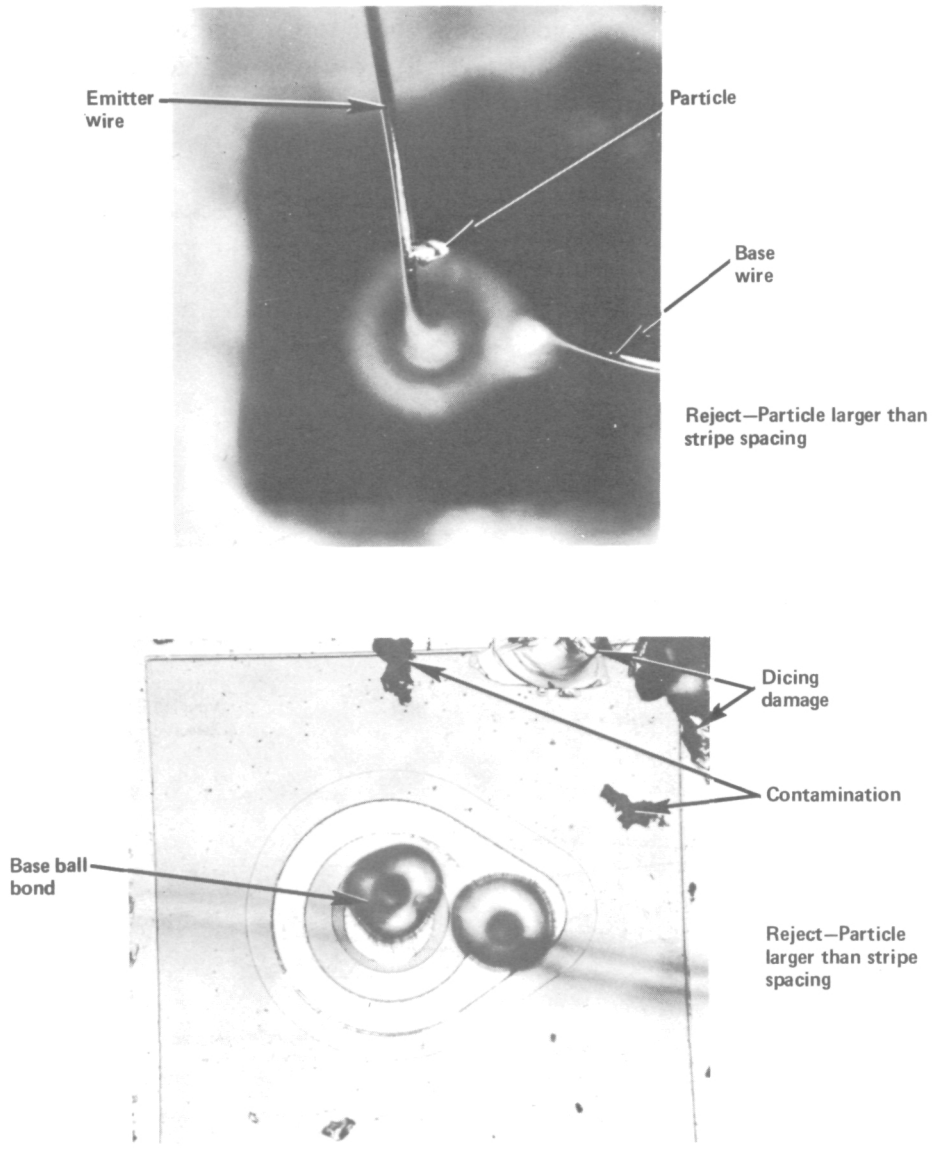
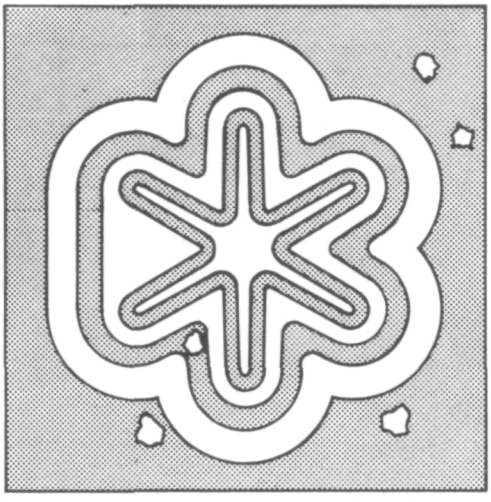
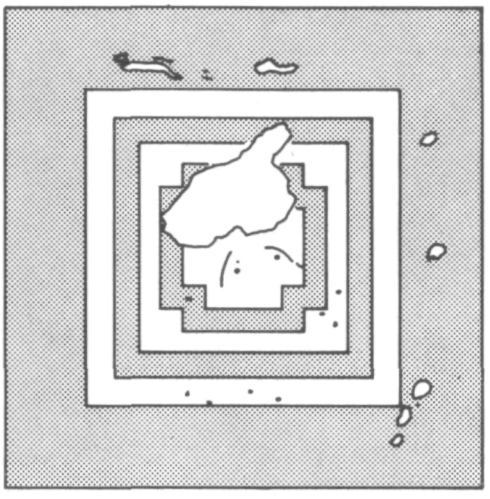


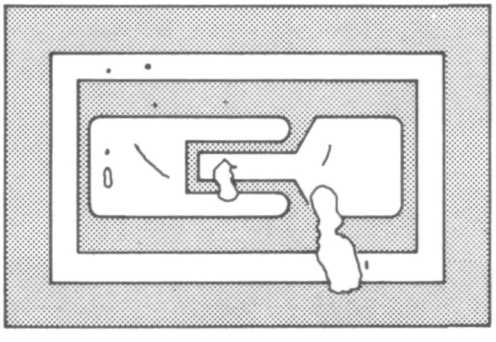
Figure 36. Particulate contamination in hybrid microcircuits.



Reject—Foreign material larger than 1 mil on die surface



Reject—Foreign material surface shorting the E-B metallization



Reject—Foreign material on die

Figure 37. Contamination in hybrid microcircuits, visual inspection criteria.

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SUMMARY

This text concerns the final preseal visual inspection of microcircuit devices to detect manufacturing defects and reduce failure rates in service. It outlines the processes employed in fabricating monolithic integrated circuits and hybrid microcircuits, discusses various failure mechanisms resulting from deficiencies in those processes, and gives the rudiments of performing final inspection. It does not discuss the experience of the inspector or the optical equipment necessary to adequately perform such inspections.

To adequately inspect high reliability devices, an inspector must be familiar with normal fabrication techniques and aware of the failure mechanisms associated with these processes. In addition, the inspector must acquire considerable experience in using microscopes and develop sufficient tolerance (of eye fatigue) to permit examination of a relatively large number of devices.

The success of final preseal visual inspection depends on both the manufacturer's motivation and the inspector's training. Deficient inspection is evident in the quality of "high reliability" devices received at Goddard Space Flight Center. This text and the accompanying course will train Goddard employees to verify that proper inspections are being made.

ACKNOWLEDGMENT

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